

*Intel's*

*8051*

*Micro controller*



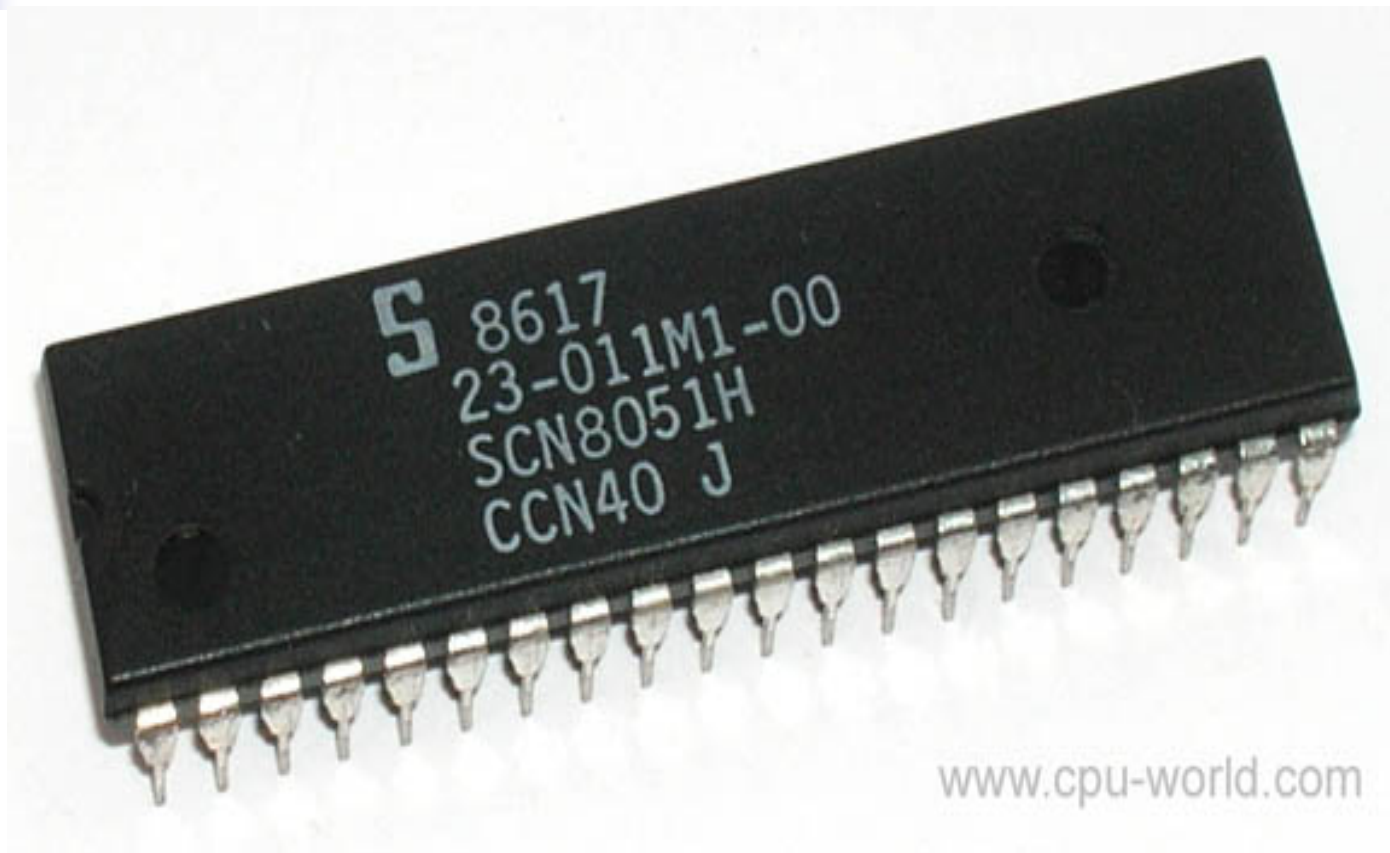
# Basics

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- What are Micro controller's ?
- Why the name Micro controller ?

Basically used for control actions. It is used to control the operation of machine using fixed program that is stored in ROM/EPROM and that does not change over the life time.

- What is MCS 51 ?
- Why to study 8051 ?





# Features of 8051

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- 8 bit ALU.
- 16 bit PC and DPTR.
- 8 bit stack pointer and 8 bit PSW.
- 4K internal ROM
- 128 bytes of Internal RAM.
- 32 bits arranged as four, 8 bit ports P0-P3.
- Two 16 bit timer/counters, T0 & T1.
- Full duplex serial Port.

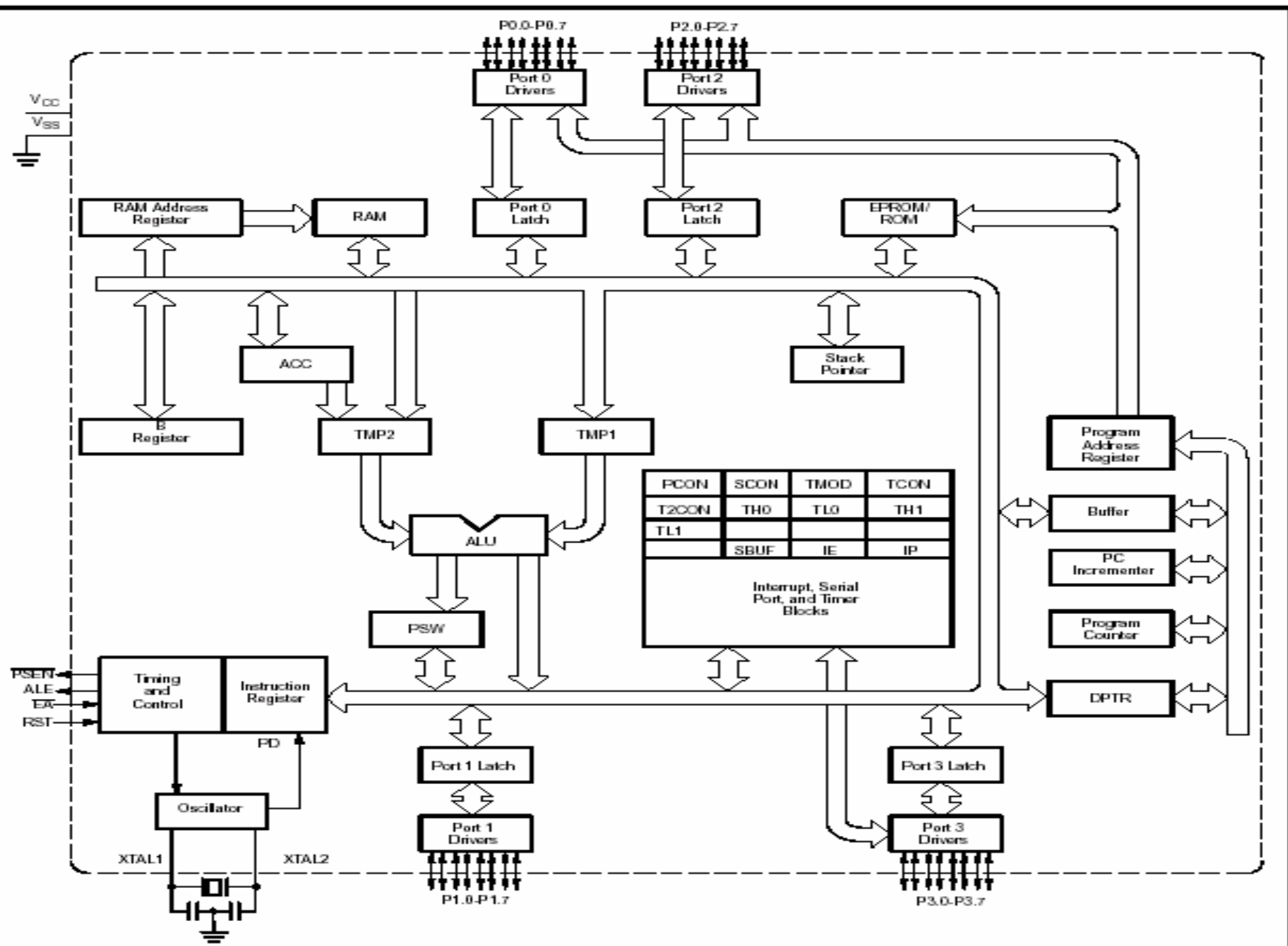


# Features contd...

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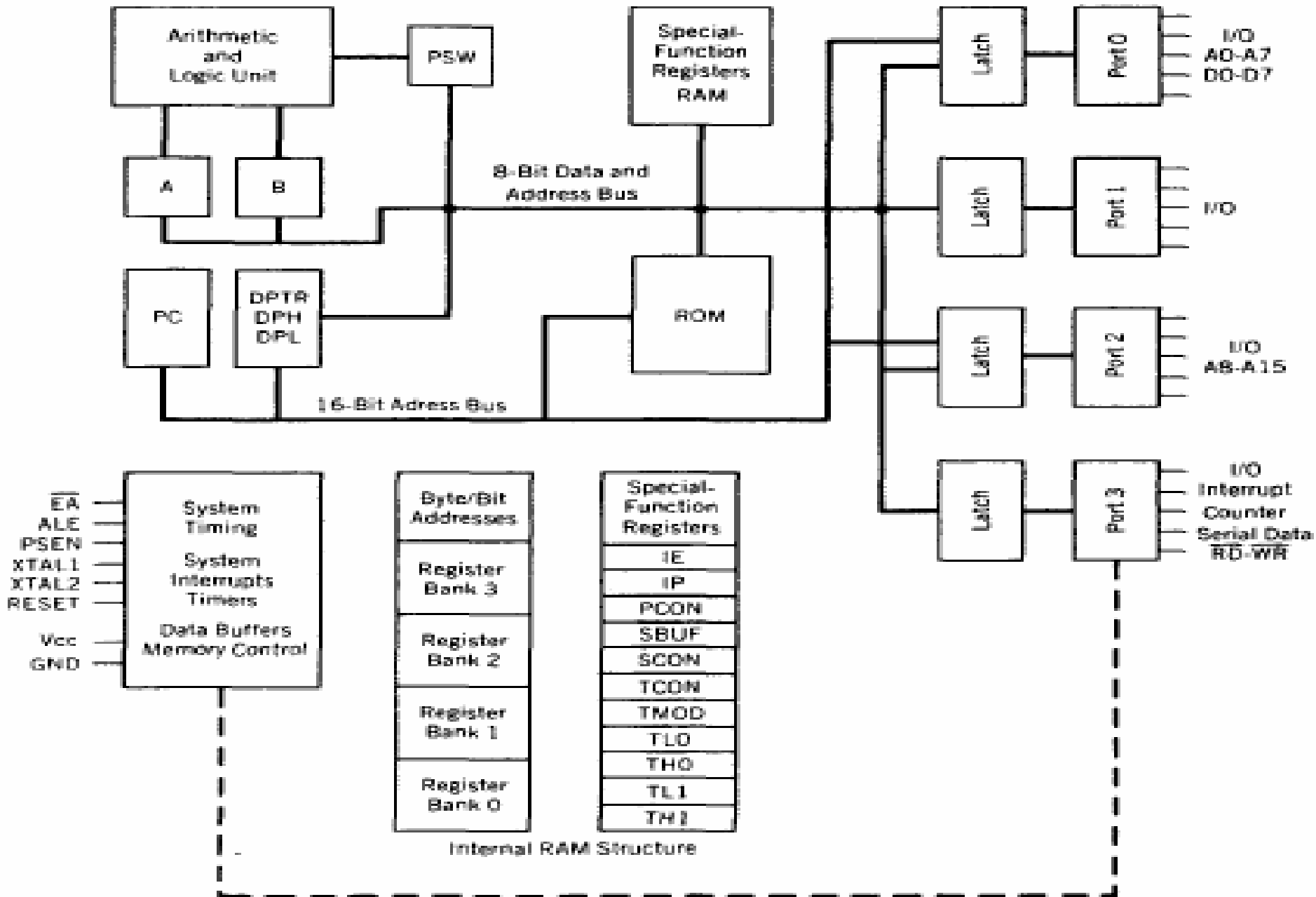
- Control Registers  
TCON, TMOD, SCON, PCON, IP, IE etc (SFR's).
- Two External and three internal interrupt sources.
- 0-12 MHz clock.
- 40 pin DIP package.
- Works in Power Down and Idle mode.
- Powerful Instruction set.

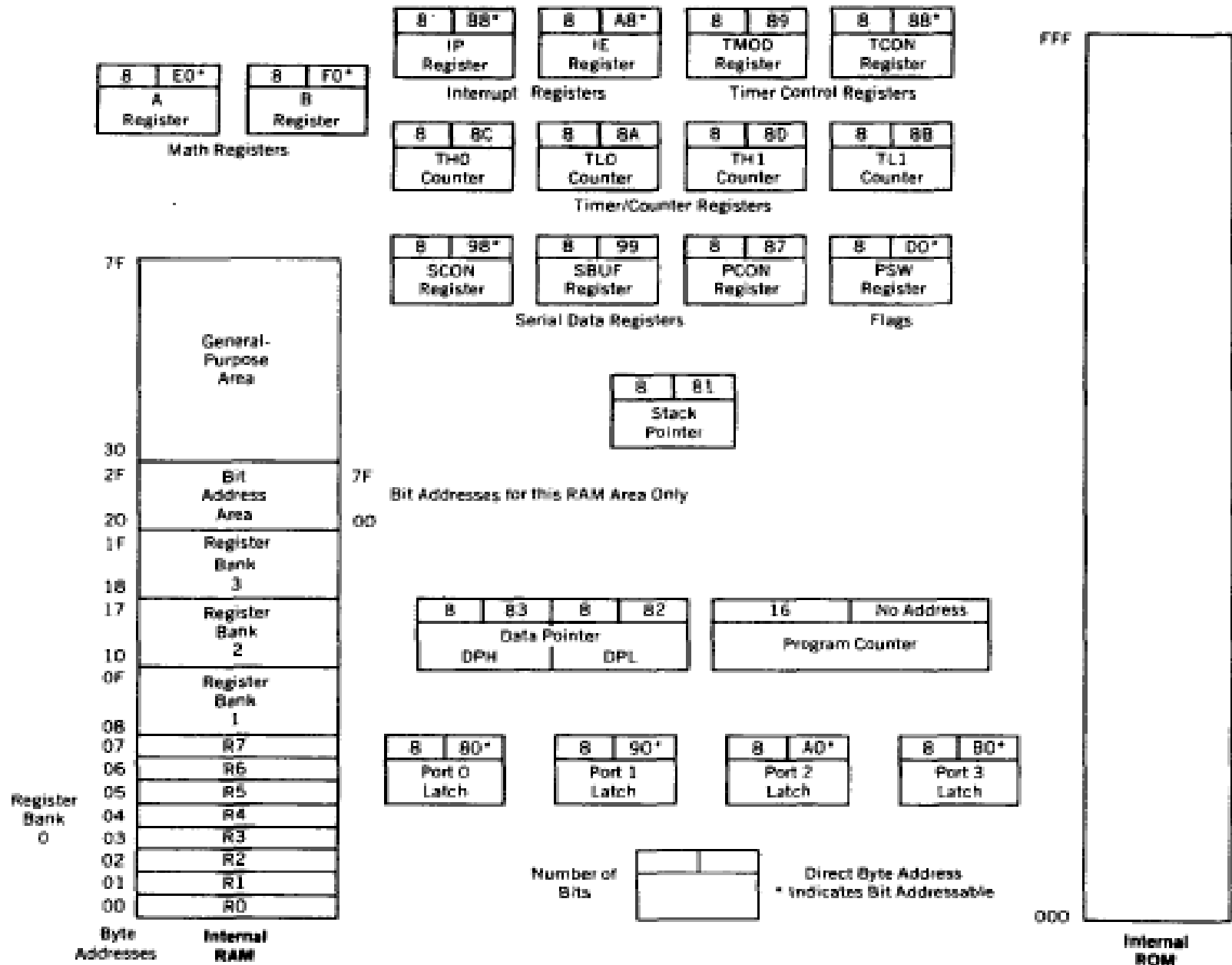
# Block Diagram of 8051.



# Pin Diagram of 8051

T2, P1.0	□ 1	40	□ VDD
T2EX, P1.1	□ 2	39	□ P0.0, AD0
RXD1, P1.2	□ 3	38	□ P0.1, AD1
TXD1, P1.3	□ 4	37	□ P0.2, AD2
INT2, P1.4	□ 5	36	□ P0.3, AD3
$\overline{\text{INT3}}$ , P1.5	□ 6	35	□ P0.4, AD4
$\overline{\text{INT4}}$ , P1.6	□ 7	34	□ P0.5, AD5
$\overline{\text{INT5}}$ , P1.7	□ 8	33	□ P0.6, AD6
RST	□ 9	32	□ P0.7, AD7
RXD, P3.0	□ 10	31	□ $\overline{\text{EA}}$
TXD, P3.1	□ 11	30	□ $\overline{\text{ALE}}$
$\overline{\text{INT0}}$ , P3.2	□ 12	29	□ $\overline{\text{PSEN}}$
$\overline{\text{INT1}}$ , P3.3	□ 13	28	□ P2.7, A15
T0, P3.4	□ 14	27	□ P2.6, A14
$\overline{\text{T1}}$ , P3.5	□ 15	26	□ P2.5, A13
WR, P3.6	□ 16	25	□ P2.4, A12
$\overline{\text{RD}}$ , P3.7	□ 17	24	□ P2.3, A11
XTAL2	□ 18	23	□ P2.2, A10
XTAL1	□ 19	22	□ P2.1, A9
Vss	□ 20	21	□ P2.0, A8



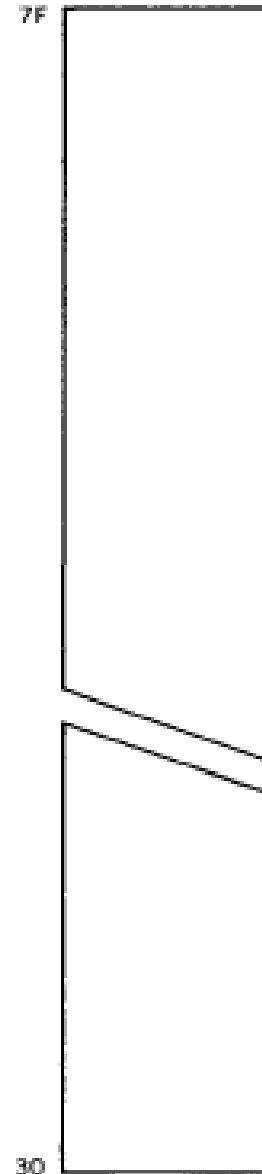


Bank 3	1F	R7
	1E	R6
	1D	R5
	1C	R4
	1B	R3
	1A	R2
	19	R1
	18	R0
Bank 2	17	R7
	16	R6
	15	R5
	14	R4
	13	R3
	12	R2
	11	R1
	10	R0
Bank 1	0F	R7
	0E	R6
	0D	R5
	0C	R4
	0B	R3
	0A	R2
	09	R1
	08	R0
Bank 0	07	R7
	06	R6
	05	R5
	04	R4
	03	R3
	02	R2
	01	R1
	00	R0

**Working  
Registers**

2F	7F	78
2E	77	70
2D	6F	68
2C	67	60
2B	5F	58
2A	57	50
29	4F	48
28	47	40
27	3F	38
26	37	30
25	2F	28
24	27	20
23	1F	18
22	17	10
21	0F	08
20	07	00

**Bit Addressable**

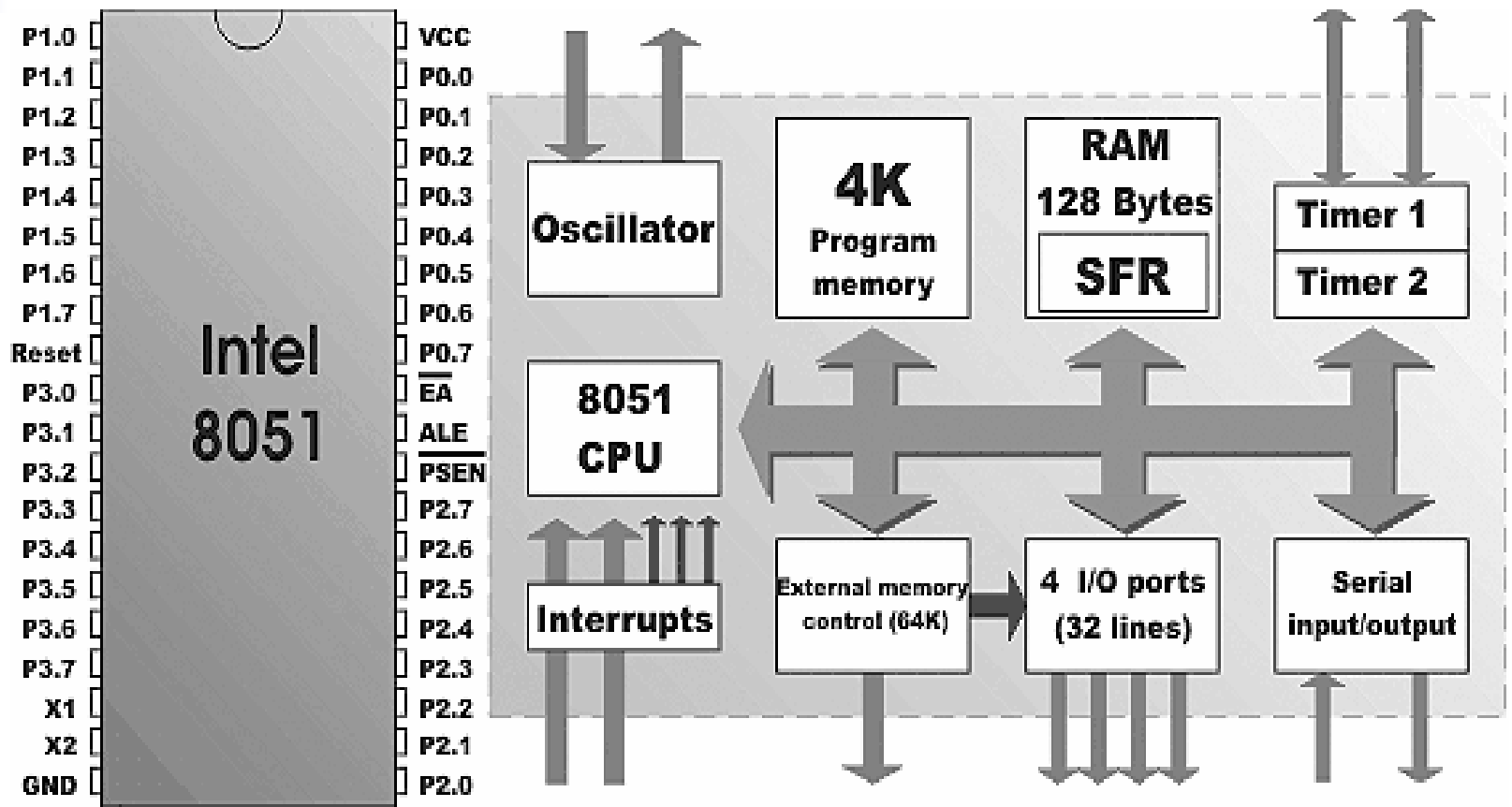
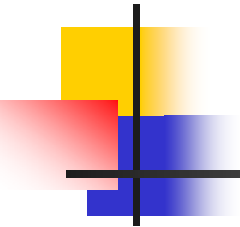


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**General Purpose**

## Internal RAM Organization





# Internal RAM Organization

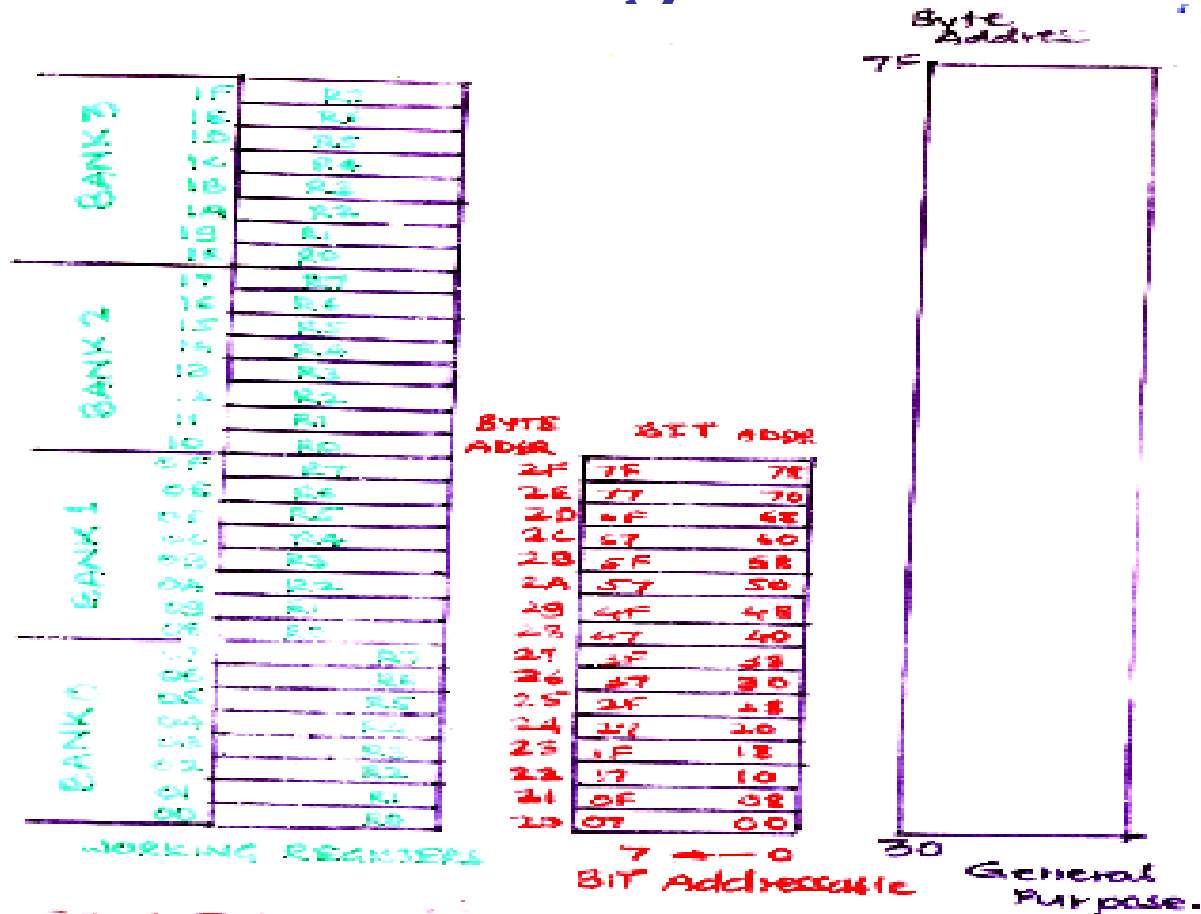
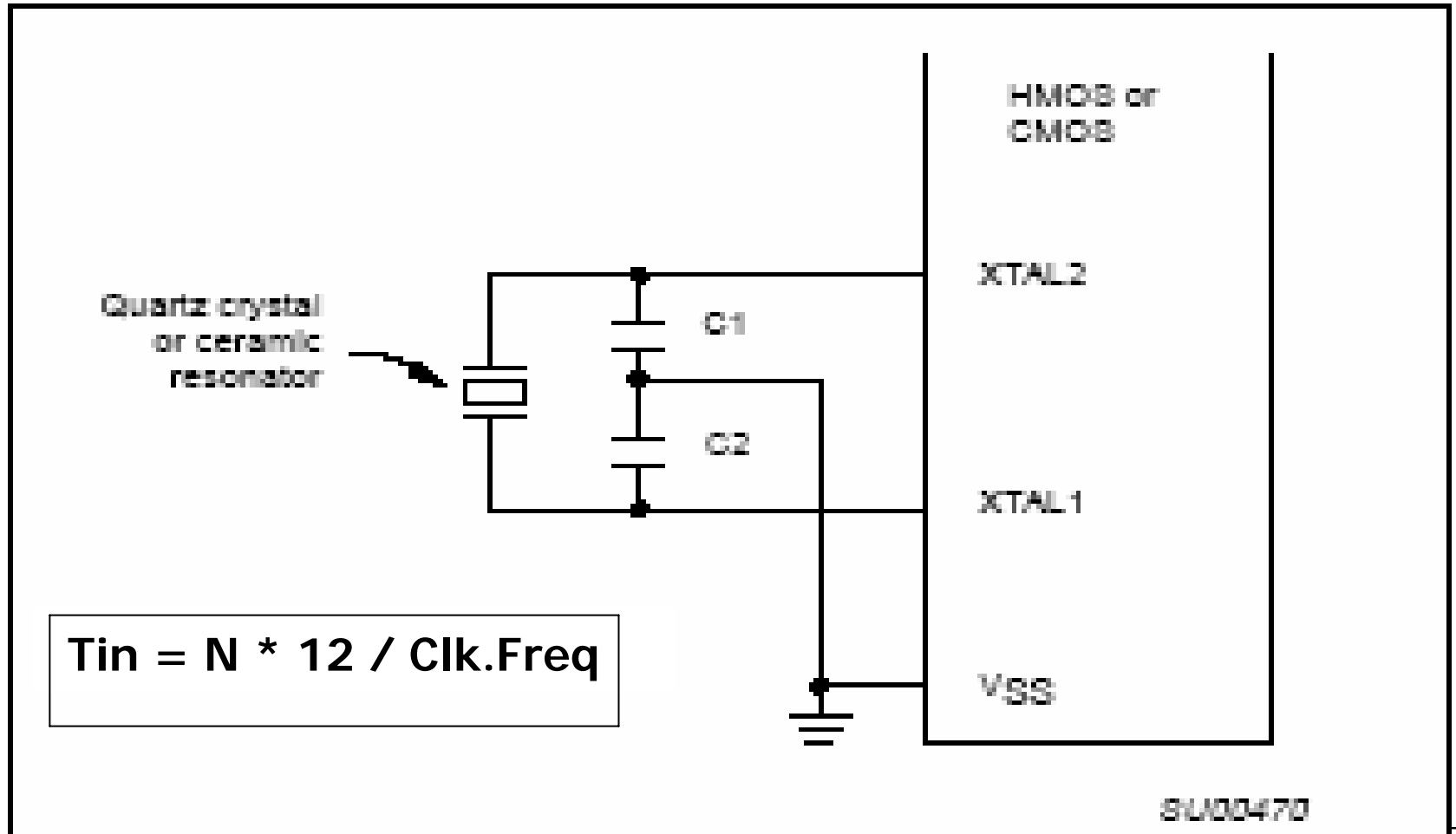


Fig-4- Internal RAM organization

# Clock for 8051.





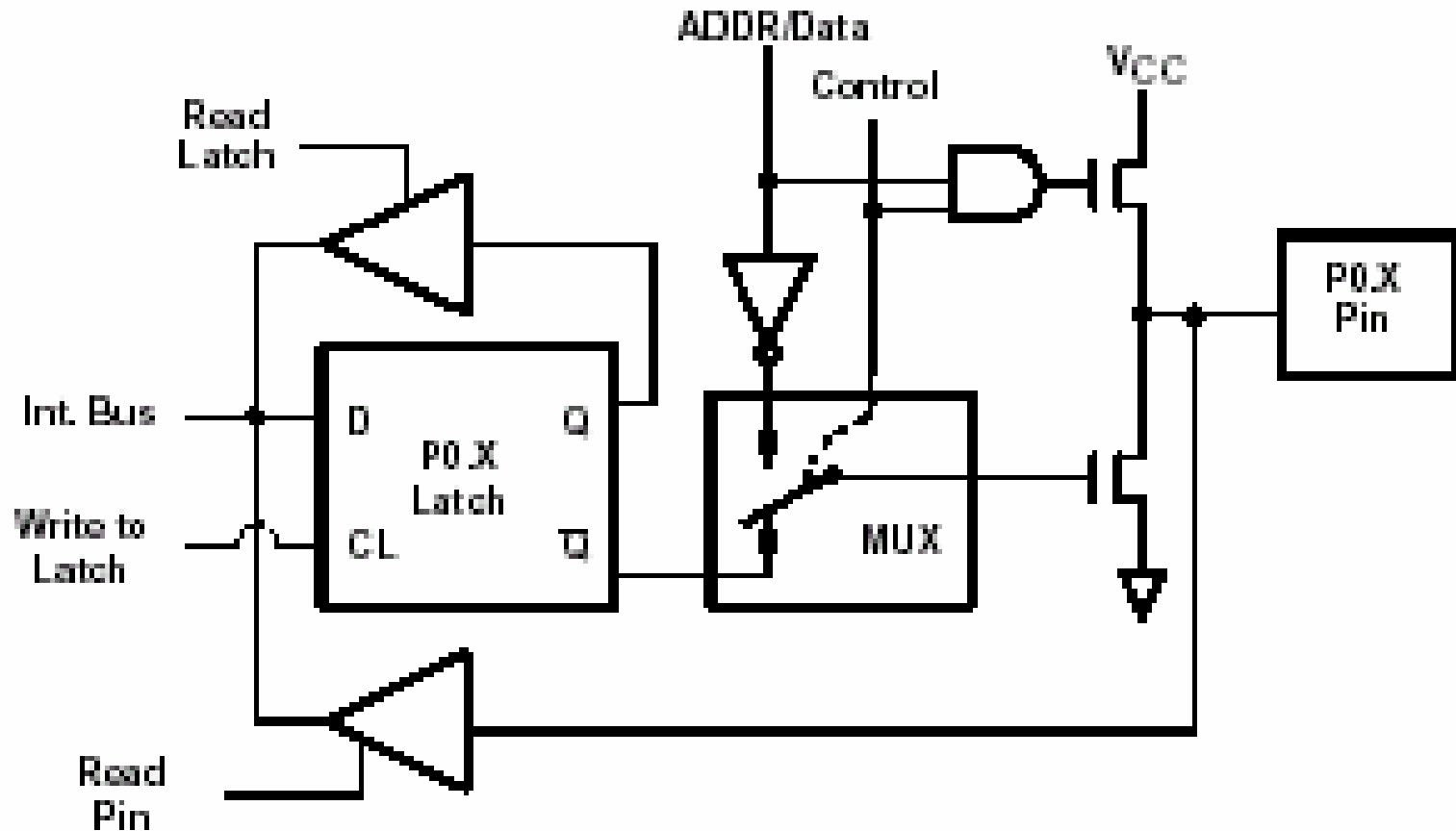
# Program Status Word (PSW)

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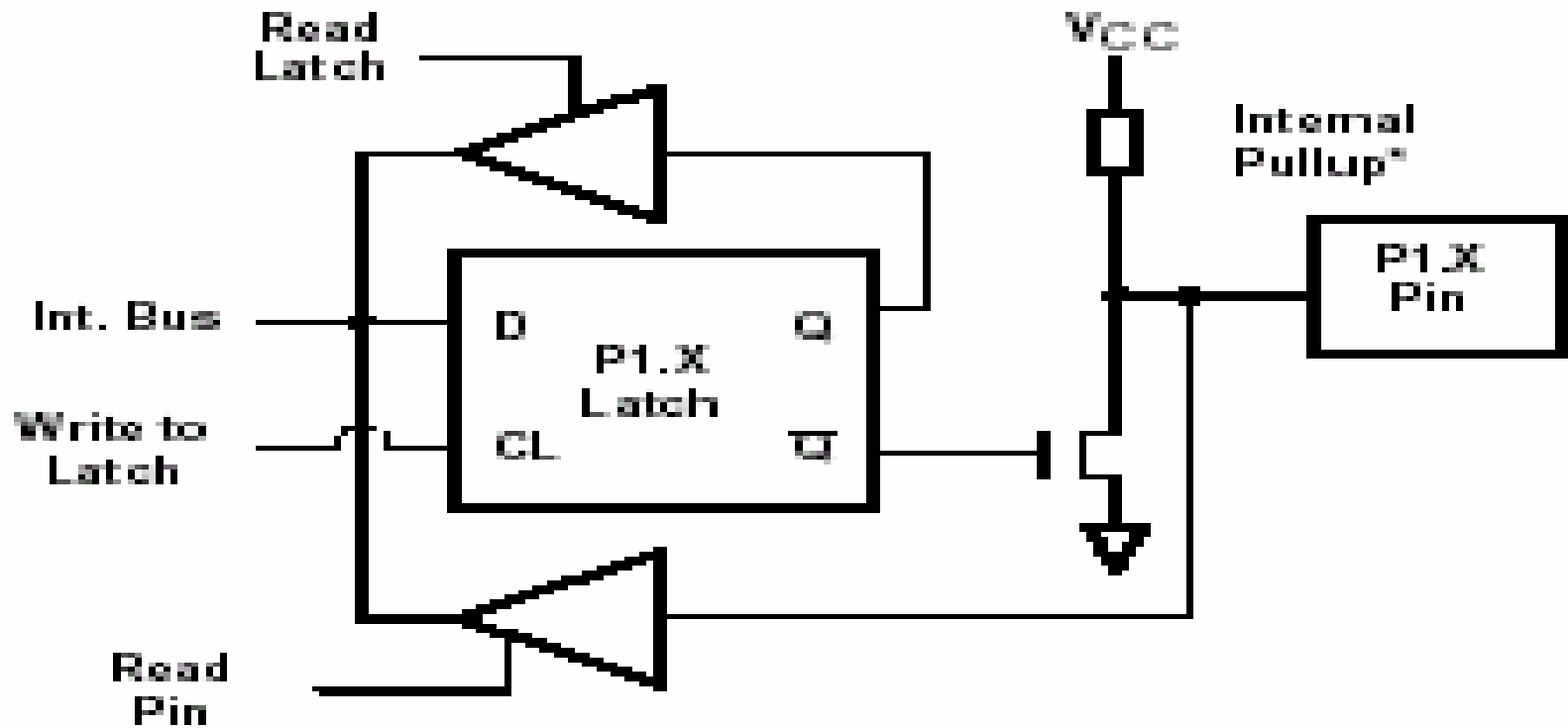
7      6      5      4      3      2      1      0

CY	AC	F0	RS1	RS0	OV	---	P
----	----	----	-----	-----	----	-----	---

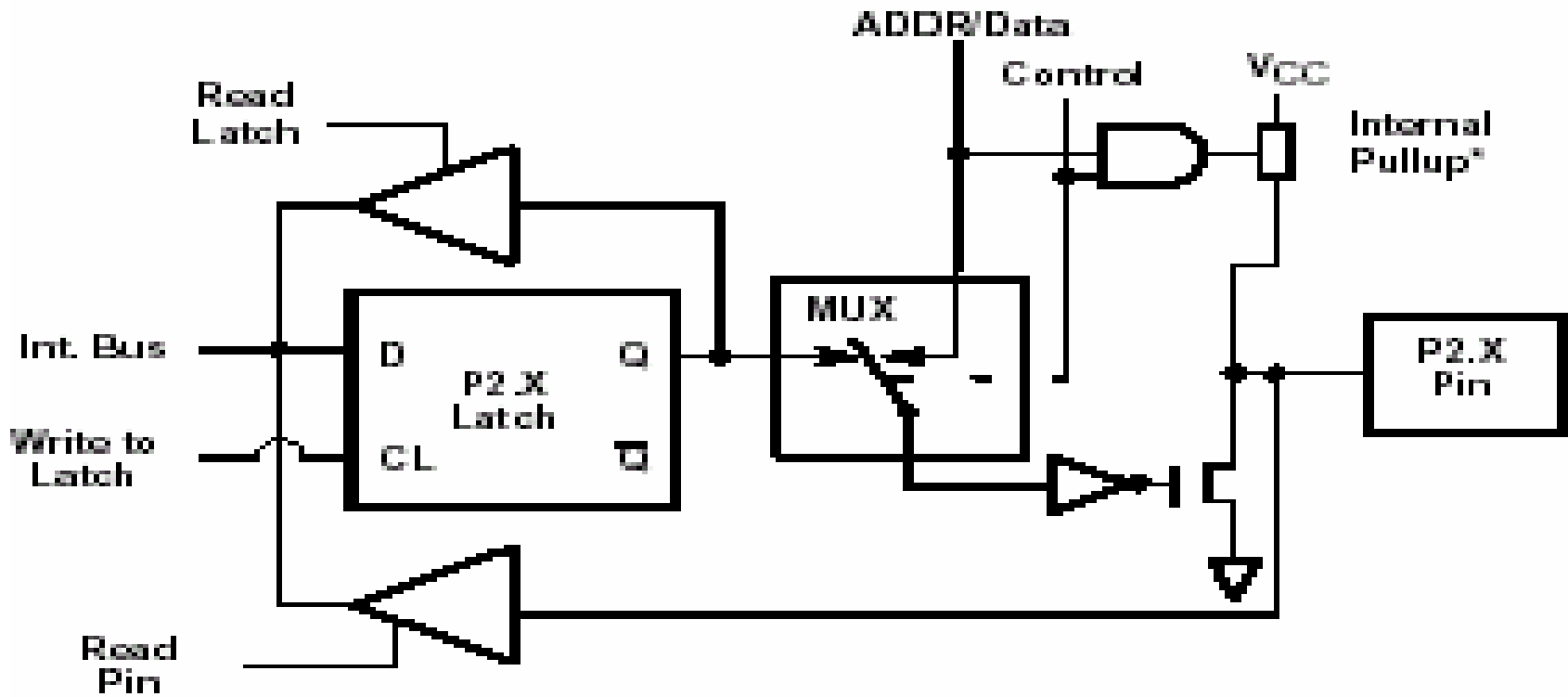
# I/O Ports of 8051-Port 0



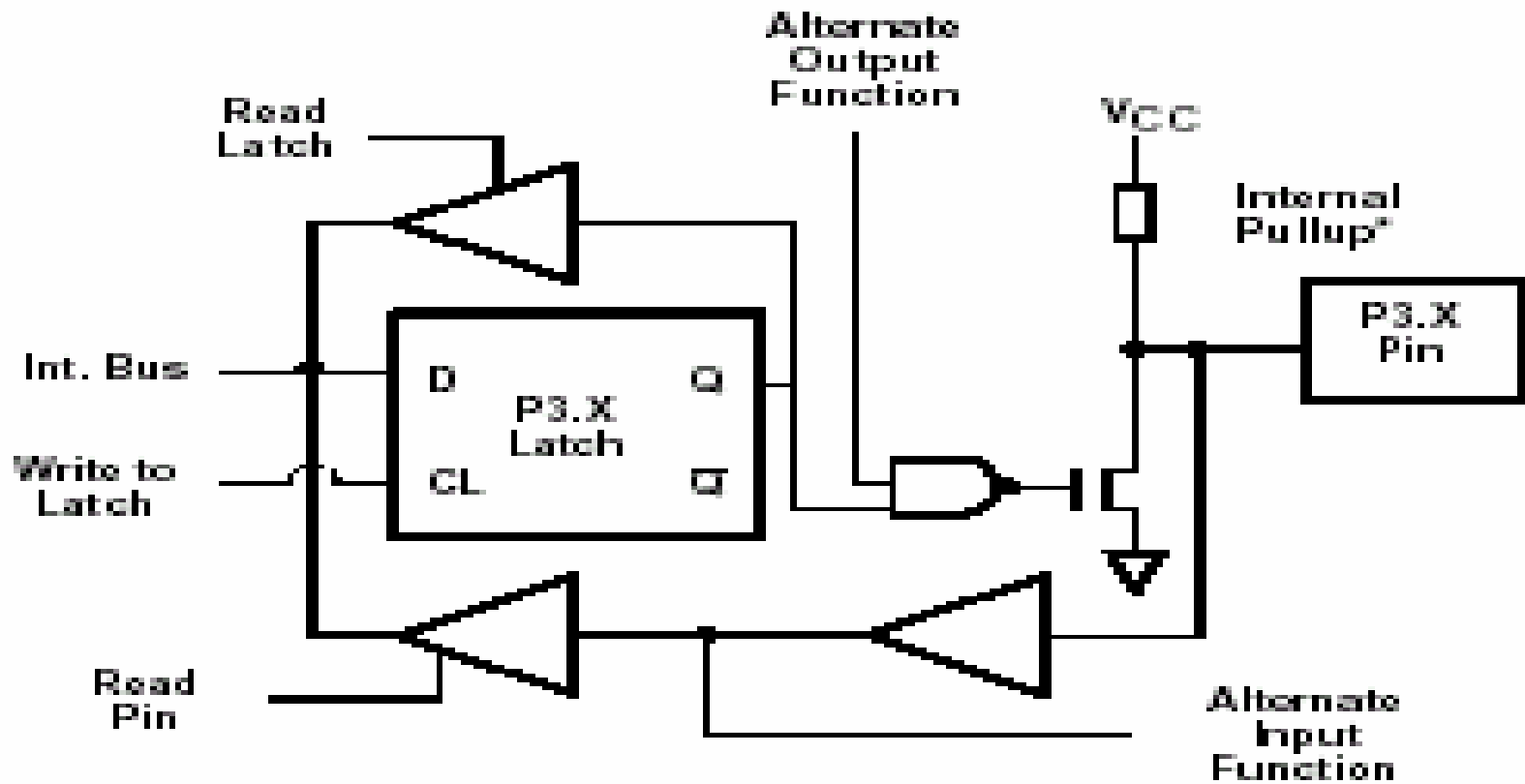
# I/O Ports of 8051-Port 1



# I/O Ports of 8051-Port 2



# I/O Ports of 8051-Port 3





# Memory Interfacing with 8051

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- How to interface Program memory(EEPROM) up to 64 KB to 8051 ?
- How to interface Data memory(RAM) upto 64 KB to 8051 ?
- How 8051 distinguishes Program and data memory operations ?



# Timer Control Register (TCON)

7	6	5	4	3	2	1	0
TF 1	TR1	TF0	TR0	IE 1	IT1	IE0	IT 0

TF1 :Vector location 001B H.

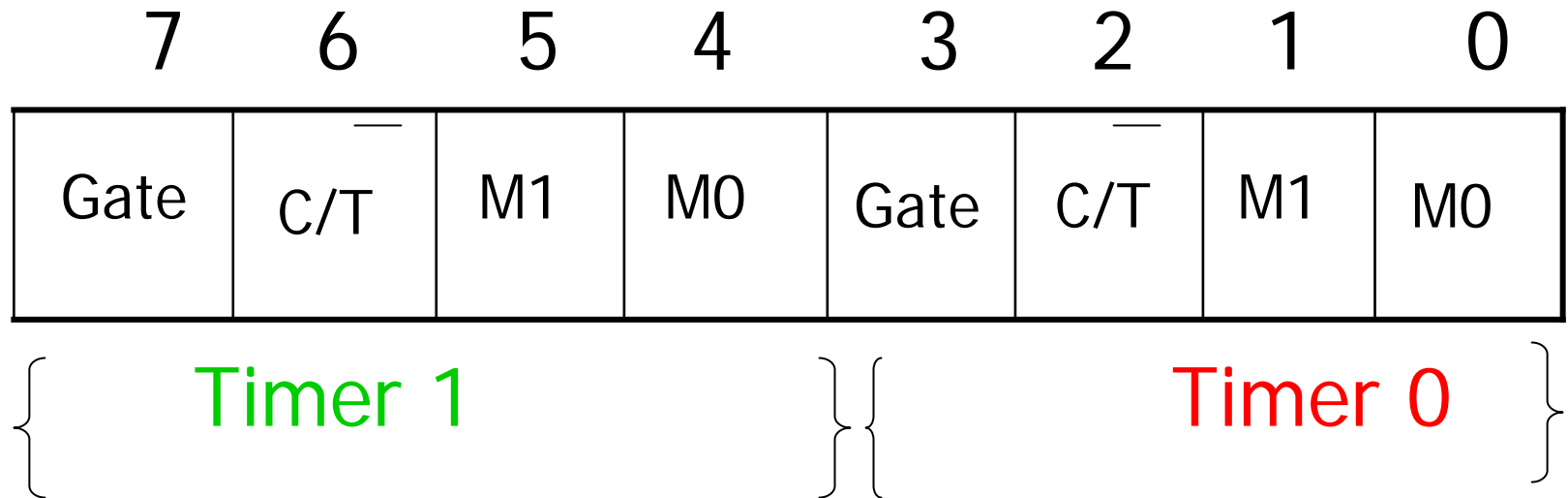
TF 0: Vector location 000B H

IE 1 : Vector location 0013 H

IE 0: Vector location 0003 H



# Timer Mode (TMOD)





# Modes of Timer/Counter

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- Mode 0 : 5 bit prescaler (13 bit )
- Mode 1 : 16 bit timer
- Mode 2 : 8 bit Auto reload
- Mode 3 : TL 0 and TH0 are independent but TH0 controlled by TR1 and TF1.



# Serial Input/Output

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- Registers used are SCON and SBUF.
- There are physically two SBUF registers having same address i.e 99 H. Interrupt is generated whenever data is transmitted and received.
- Controller goes to execute ISR for serial communication from 0023h.



# Serial Control (SCON) register

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM0    SM1

0      0      Shift register mode  
              baud=1/12

0      1      8 bit UART baud=variable

1      0      9 bit UART baud= f/32 or f/64

1      1      9 bit UART baud = variable



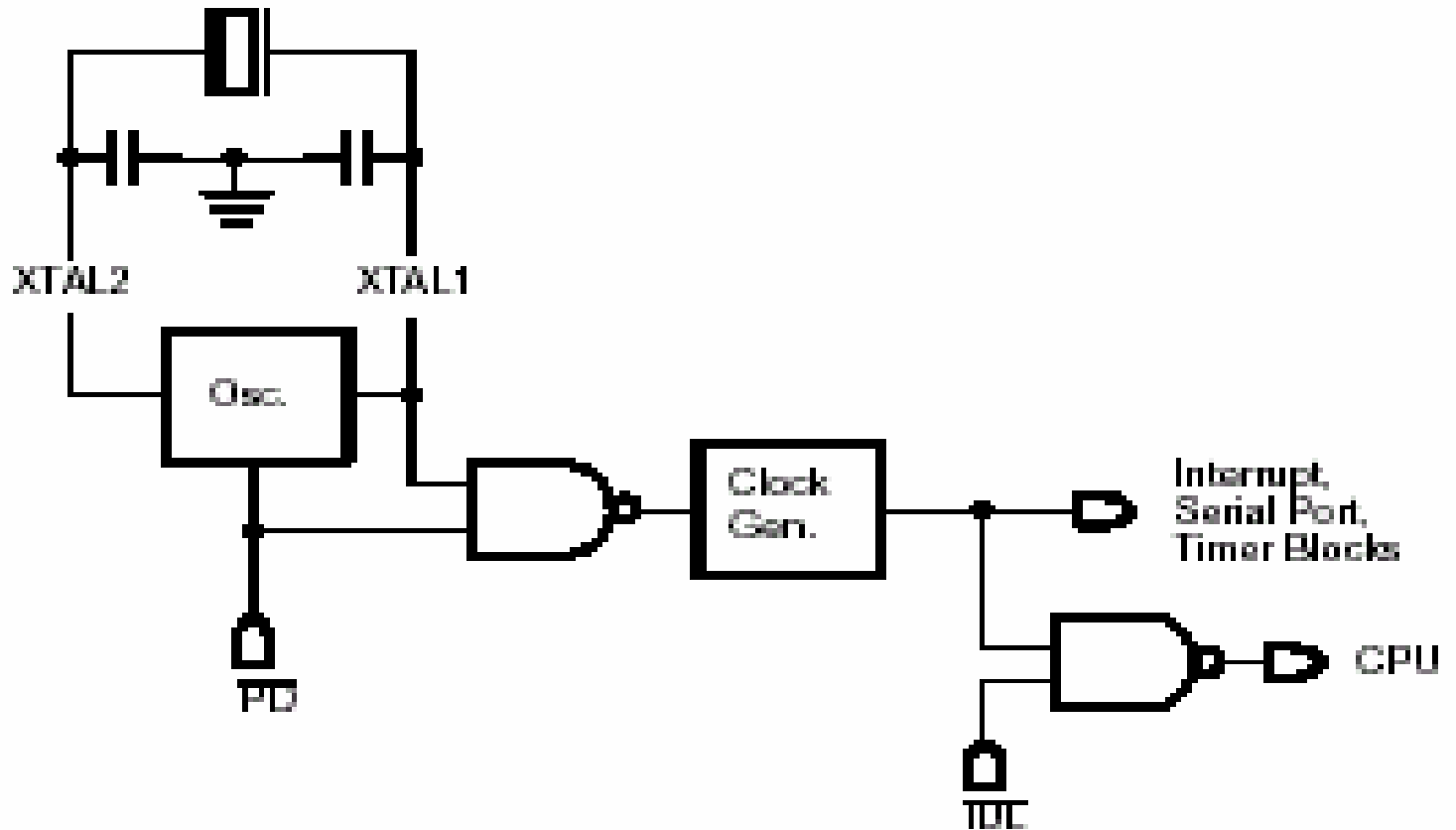
# Power Control (PCON) Register

7	6	5	4	3	2	1	0
SMOD	-	-	-	GF1	GF0	PD	IDL

**IDLE Mode** :The internal clock is gated off to the CPU, but not to the timer, serial port and all registers maintain the data.

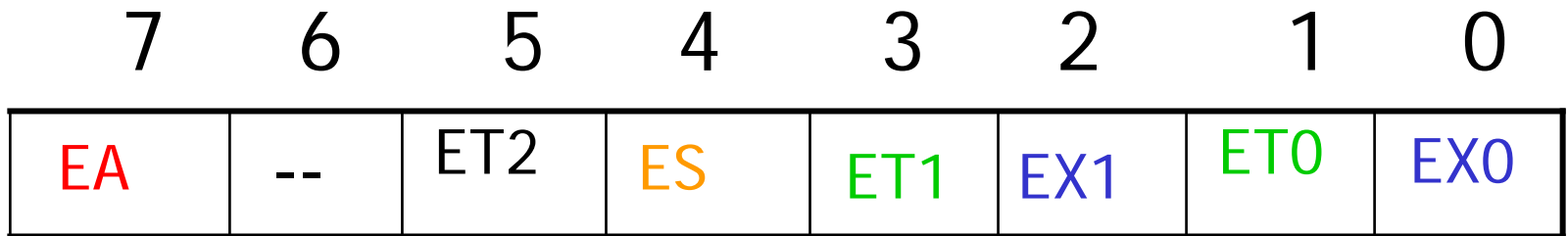
**POWER DOWN** :On chip oscillator is stopped. But RAM and SFR's are held.

# Idle and Power Down Hardware



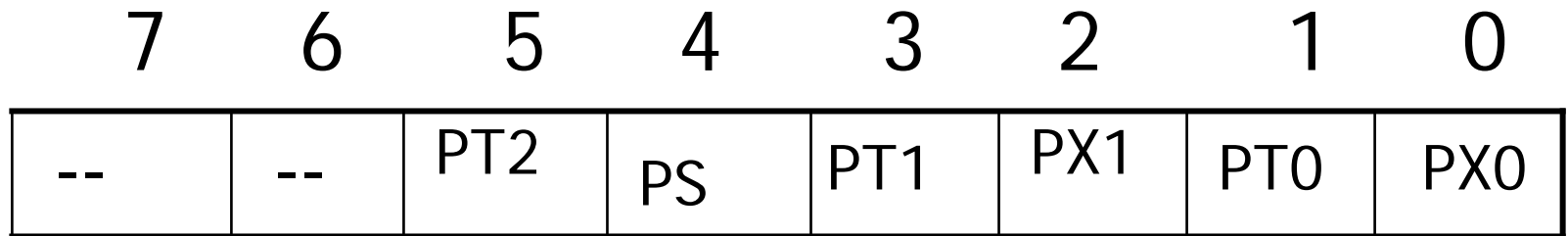


# Interrupt Enable (IE) Register





# Interrupt Priority (IP) Register



**THANK YOU**