



## PRASAD D. KHANDEKAR

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<b>Education and Experience:</b>	<ul style="list-style-type: none"><li>• B.E. (Industrial Electronics) University Of Pune 1992</li><li>• M.E (Electronics) Shivaji University 2004</li><li>• PhD Thesis submitted ( Low Power VLSI )</li><li>• Teaching Experience : 14 years</li><li>• Industry Experience: 5 years</li></ul>
<b>Research Interests:</b>	Low Power VLSI Design <ul style="list-style-type: none"><li>• CMOS Circuits (Power Estimation and Delay estimation)</li><li>• Custom IC Design</li><li>• Energy recovery adiabatic logic</li></ul>
<b>Tools known:</b>	<ul style="list-style-type: none"><li>• Cadence Custom IC Design Package: ICFB, VIRTUOSO, ASSURA,</li><li>• Simulation: SPECTRE,HSPICE</li><li>• Text editor for technical writing: LaTeX tools like TeXNic Center and MikTeX2.8</li></ul>
<b>PhD Work:</b>	<ul style="list-style-type: none"><li>• Registered for PhD in January 2007</li><li>• Guide: Dr Mrs. S Subbaraman</li><li>• Title: Low Power Digital Design Using Energy Recovery Adiabatic Logic.</li></ul>
<b>Patent:</b>	<ul style="list-style-type: none"><li>• One patent published in ‘The Patent Office Journal’ dated 02/12/2011 page number 22273.</li><li>• One patent is being filed.</li></ul>
<b>Research Paper Publications:</b>	<ul style="list-style-type: none"><li>• International Journals: 4</li><li>• International Conferences (abroad): 4</li><li>• International Conferences (India): 3+1*</li><li>• National Conferences : 3</li></ul>

<b>Reviewer Assignments</b>	<ul style="list-style-type: none"> <li>• “The Integration” journal, the VLSI journal of Elsevier, USA No of journal papers reviewed: 02</li> <li>• “IJ-DATICS” journal UK No of journal papers reviewed: 02</li> <li>• “Journal of Engineering and Computer Innovations” No of journal papers reviewed: 01 pending</li> <li>• “International Conference at China 2010” No of papers reviewed: 01</li> <li>• “International Conference at Dhule 2011” No of papers reviewed: 01</li> <li>• “International Conference at IMECS, Hongkong” No of papers reviewed:02</li> </ul>
<b>Funded Research Projects:</b>	<ul style="list-style-type: none"> <li>• Sponsoring Agency: University Of Pune</li> <li>• Amount Rs 2,50,000/- (US\$5000 approximately)</li> <li>• Project: Estimating Power Dissipation in VLSI Circuits and Reducing It By Using Energy Recovery Adiabatic Technique</li> <li>• Status: First year progress report submitted and audited</li> </ul>
<b>Books Published:</b>	<ul style="list-style-type: none"> <li>• Two as single author</li> <li>• Seven books co-authored.</li> </ul>
<b>Award:</b>	<ul style="list-style-type: none"> <li>• Best Teacher – E&amp;TC for the year 2008-2009</li> <li>• Nominated for the national award, 'Best Low Cost Technology for the Cause of the Disabled' given away by the Ministry of Social Justice and Empowerment, Government of India in 2004</li> </ul>
<b>Other:</b>	<ul style="list-style-type: none"> <li>• Program committee member of international conference IMECS 2010,11,12 organized by IAENG at Hongkong and DATICS-NESEA 2010 Suzhou, China,</li> <li>• Invited talks on Low Power VLSI Design at many institutes.</li> </ul>

### **Research papers published as a first author**

#### **Papers published in Journals**

1. P D Khandekar et al, “Optimal Conditions for Ultra Low Power Digital Circuits”, *Journal of Active and Passive Electronic Device, USA*, 2011, Vol 6, pp 157-167
2. P D Khandekar et al, “Low power Digital Design Using Energy-Recovery Adiabatic Logic”, *International Journal of Engineering Research and Industrial Applications*, pp 199-205, 2008.

3. P D Khandekar , S Subbaraman, and R S Talware, “Ultra-Low Power Quasi-Adiabatic Inverter”, *International Journal of Computational Intelligence Research & Applications*, presented in *ICVCom’09*, SAINTGITS COE, Kottayam, Kerala, 16-18 April 2009, Vol.3,No.1, Jan-Jun 2009, pp 11-15.
4. P D Khandekar, S Subbaraman, Manish Patil, and Abhijit Chitre, "Low Power Inverter and Barrel Shifter Design Using Adiabatic Principle", *Advances in Computational Sciences and Technology (ACST)*, Vol. 3, No. 1 (2010), pp 57-65.

**Papers presented/published in International Conferences (abroad)**

1. P D Khandekar , and S Subbaraman, “Achieving Sub-Adiabatic Energy Dissipation by Varying  $V_{BS}$ ”, *International Conference ECTI-CON 09*, Pattaya, Thailand, 6-8 May 2009,978-1-4244-3388-9/09 © 2009 IEEE, pp600-603.
2. P D Khandekar , S Subbaraman, and Venkat R Vinjamoori, “Quasi-Adiabatic 2X2 Barrel Shifter”, *Fourth IEEE International Conference ICIS-2009*, University of Peradeniya, Srilanka, 29-31 December 2009, ISBN 978-1-4244-4837-1/09, IEEE catalog number:CFP0958A
3. P D Khandekar , S Subbaraman, and Achint Sharma, “Implementation and Analysis of VCO Based Power-Clock Supply Generator”, *Fourth IEEE International Conference ICIS-2009*, University of Peradeniya, Srilanka, 29-31 December 2009, ISBN 978-1-4244-4837-1/09, IEEE catalog number:CFP0958A
4. P D Khandekar, S Subbaraman, “Implementation and Analysis of Quasi-Adiabatic Inverters”, *Proceedings of the International Conference IMECS 2010*, Hongkong, 16-17 March 2010, Vol. II, pp 1348-1351

**Papers presented/published in International Conferences (India)**

1. P D Khandekar et al “Optimizing 2:1 MUX for Low Power Design Using Adiabatic Logic”, *International Conference on VLSI Design and Embedded Systems (ICVLSI’08)*, VEC, Chennai, 14-16 February 2008, pp.145-150.
2. P D Khandekar , and S Subbaraman, “Implementation of Low Power 2:1 MUX for Barrel Shifter”, *International Conference on Emerging Trends in Engineering and Technology (ICETET’08)*, G H Raisonni, Nagpur, 16-18 July 2008, 978-0-7695-3267-7/08 © 2008 IEEE, pp 404-407
3. P D Khandekar , S Subbaraman, and A. Sharma, “A VCO Based Power-Clock Supply Generator for Quasi-Adiabatic Circuits”, *International Conference WECON-2009*, Chitkara IET, Punjab, 23-24 October 2009, Embedded Systems Vol. II, pp 55-58
4. Amit Kenjale, P D Khandekar and A V Chitre, “Design and Implementation of Power-clock Generation” is accepted by *International Conference ICDCS’12*, Karunya University, Coimbatore, India for presentation publication and will be indexed by IEEEExplore
5. Amruta Kulkarni and P D Khandekar, “Design and Implementation of Low Power Cloack Distribution Network” in *International Conference ICAESM’12*, EGA Pillay Engineering College, Nagapattinam, India. for presentation publication and will be indexed by IEEEExplore.

**Papers presented/published in National Conferences/ seminars / symposia**

1. Prasad Khandekar et al , “Adiabatic Logic ”, *National conference on Recent Trends in Technology RTIT06* , Jalgaon, December 2006

2. Prasad Khandekar et al , “Efficiency of Adiabatic Logic for Low Power Design”, *National conference on Emerging Trends in Electronics NETE06* , MAE Alandi, Pune, 28<sup>th</sup> & 29<sup>th</sup> December 2006
3. Prasad Khandekar et al, “Fuzzy Logic for Automatic Tuning of Myoelectric Prosthesis”, *National conference on Emerging Trends in Biomedical Engineering BIOCON05*, BVDU, Pune, September 2005.

**References:**

1. **Dr (Mrs) Shaila Subbaraman**  
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2. **Dr D Nagchoudhury**  
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