

PIC

Microcontroller



What is PIC ?

- **P**eripheral **I**nterface **C**ontroller from Microchip Technology Inc.USA.
www.microchip.com
- PIC 16c6x/16c7x is used for learning purpose.
- PIC 18Fxx is also popular and widely used series today.



Features of 16C6x/7x family.

- Family includes controllers from 16c61/62/64/71/74/710/715 etc.
- They are **RISC** processors and uses **Harvard** architecture.
- Different bus widths of data and program memory. Data memory is 8 bit wide where as program memory is 12, **14**, 16 bits wide. The instruction holds immediate data along with instruction code.



Features Contd..

- Only **35** instructions.
- Most instructions take 0.2 microseconds to execute when operated at 20 MHz.
- Machine cycle consist of 4 clock pulses.
- Instruction set is highly **orthogonal**.
- 1-3 Timers with 8/16 bit prescalar.
- Watch Dog timer (**WDT**)
- 13-33 I/O pins.



Features Contd..

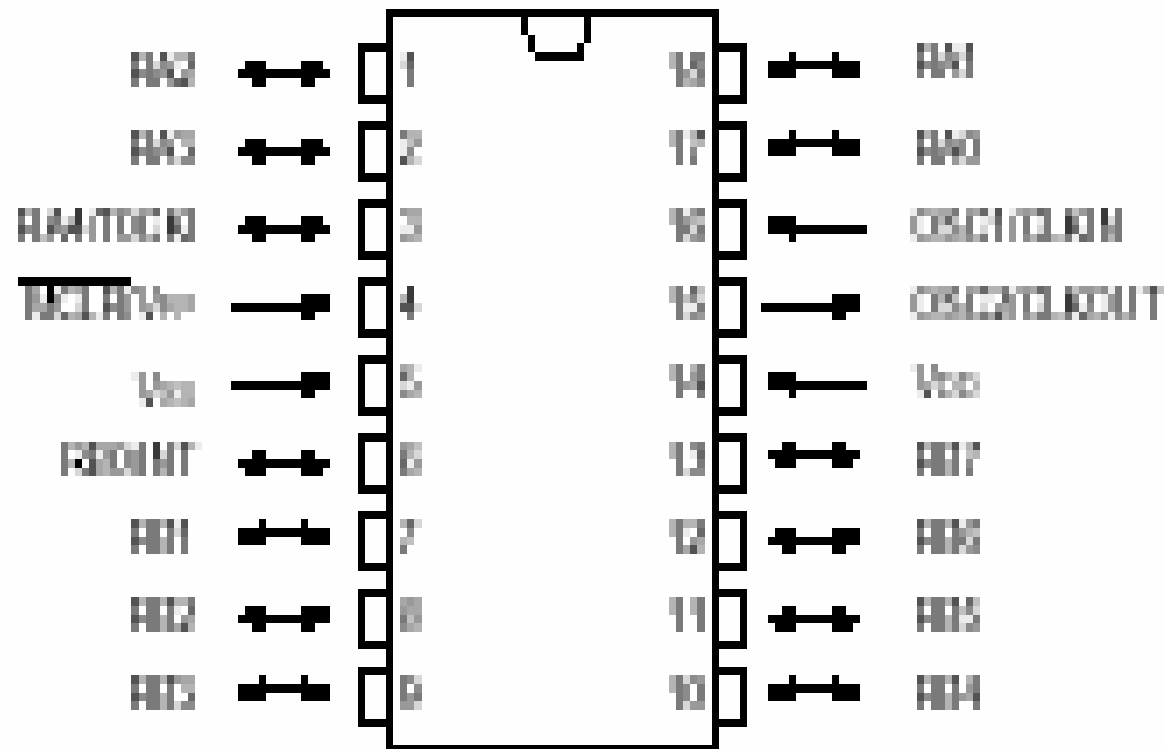
- 3-12 interrupt Sources.
- 4/8 Channel, 8 bit on chip ADC.
- Power on Reset. (POR)
- Brown out Reset (**BOR**).
- Capture/Compare/ PWM modules.
- USART
- Synchronous serial port (SSP) with SPI and I2C.
- Power saving SLEEP mode.



Features Contd..

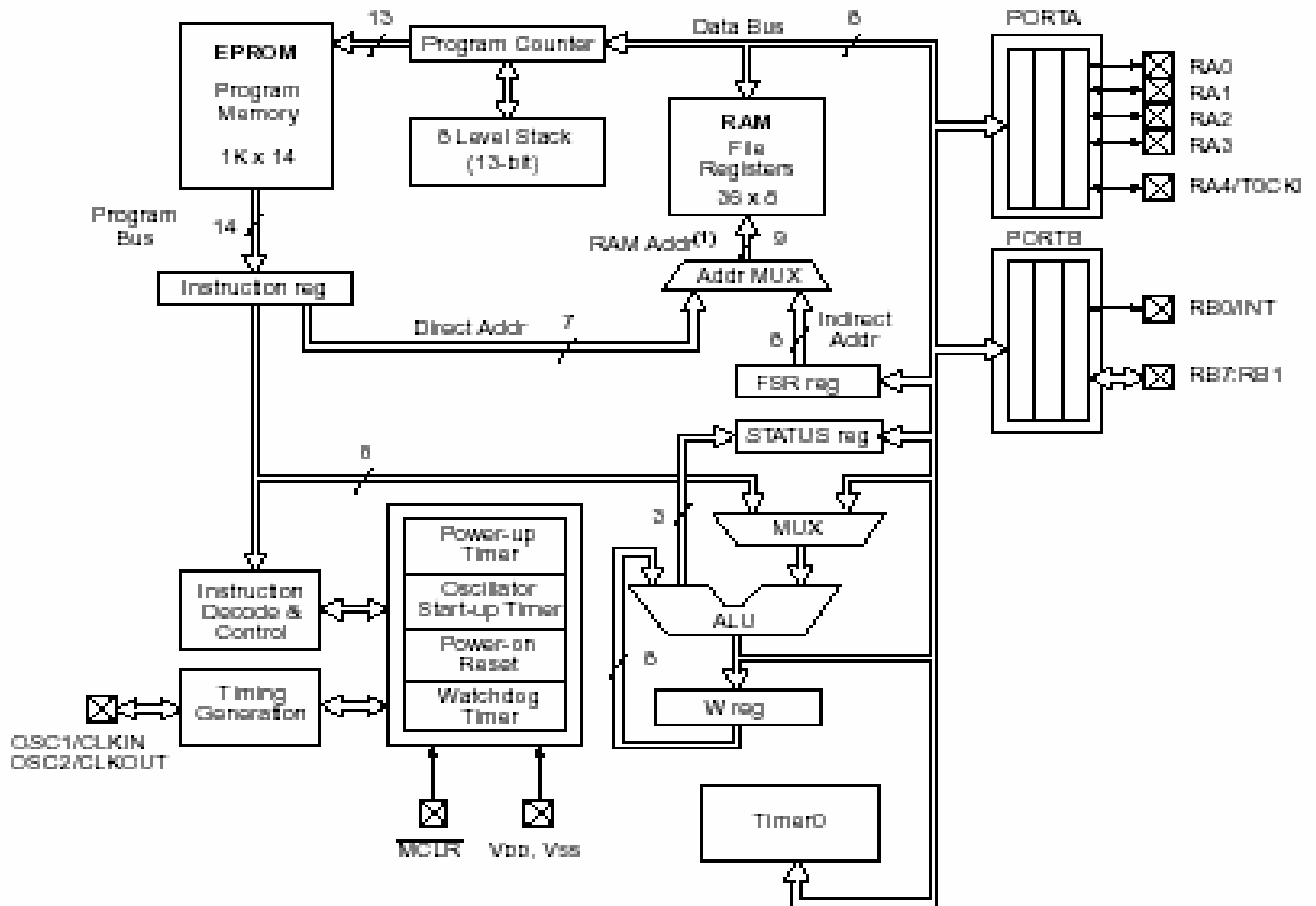
- Wide operating Voltage range 2.5 V to 6.0 V. Very Low power consumption.
- Commercial, Industrial and Extended Temperature ranges.
- Parallel slave port (PSP), 8 bits wide with external RD, WR and CS controls.

PDIP, SOIC, Windowed CERDIP



PIC16C61

PIC Internal Architecture





PIC Architecture

- **ALU**

Size is 8 bit

Performs operations with temporary working register and (W register) and any register file.

- **W register**

8 bit wide. It contains one of source operands during execution of instruction and may serve as the destination for the result of operation.

Used only for ALU operations.



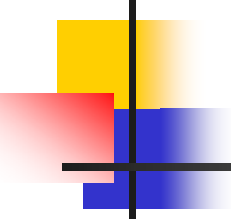
Architecture Continued...

- STATUS Register

7	6	5	4	3	2	1	0
0	0	RPO	$\overline{T0}$	\overline{PD}	Z	DC	C

C = Carry Bit

DC = Digits Carry (Same as AC)

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- Z = Zero
 - TO = Reset status bit (Time out bit)
 - PD = Reset status bit (Power down)

These bits are used along with SLEEP mode. After coming out from SLEEP processor checks these bits to determine which kind of event is responsible for bringing out of SLEEP mode.

- RPO = Register Bank Select bit. If 0 selects bank 0 otherwise bank 1.



Architecture Contd..

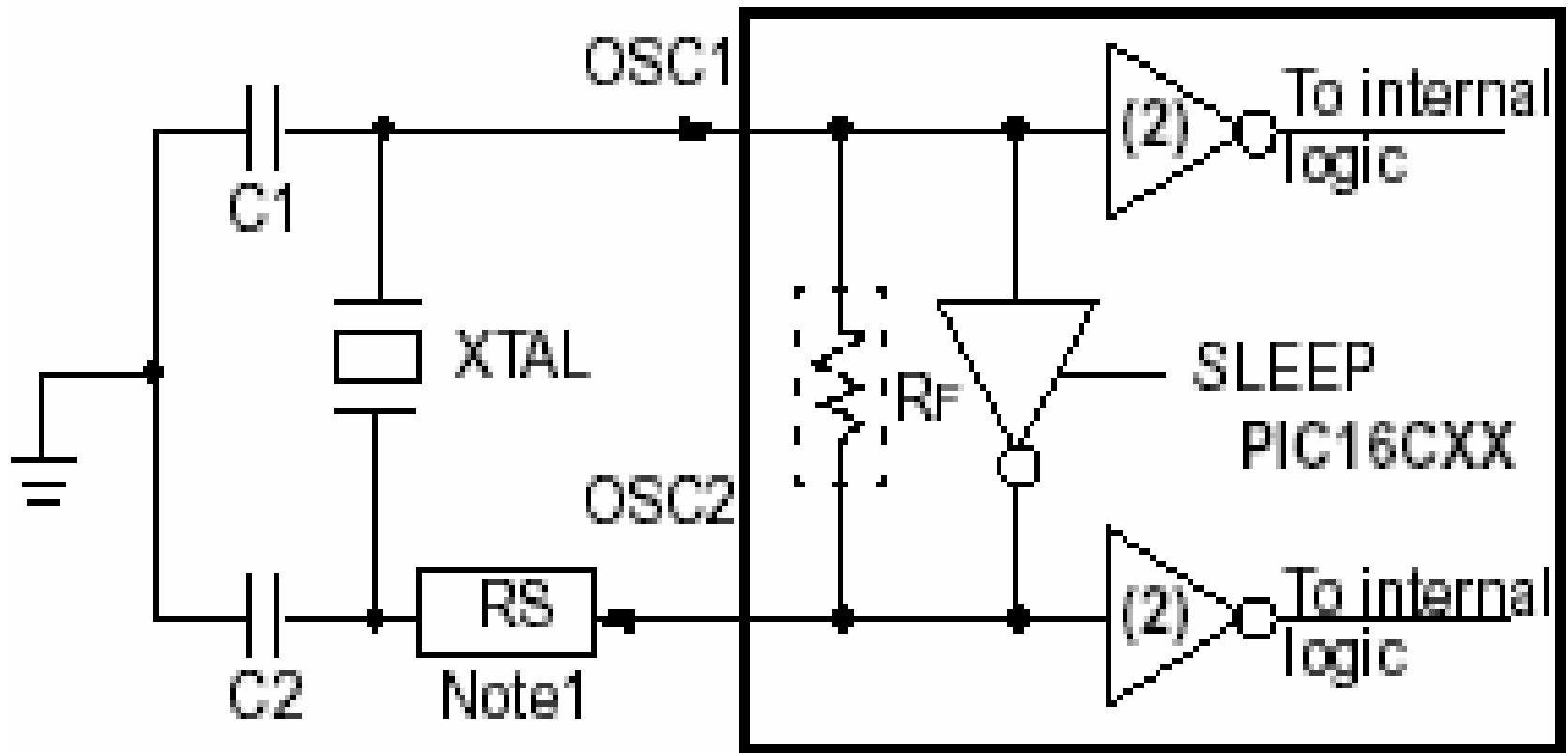
- **FSR** Register (File Selection Register)
FSR is a pointer used for indirect memory addressing in the whole register file. In indirect addressing mode one has to write address byte in FSR and then use **INDF** (Indirect thro FSR).INDF is used in instruction.



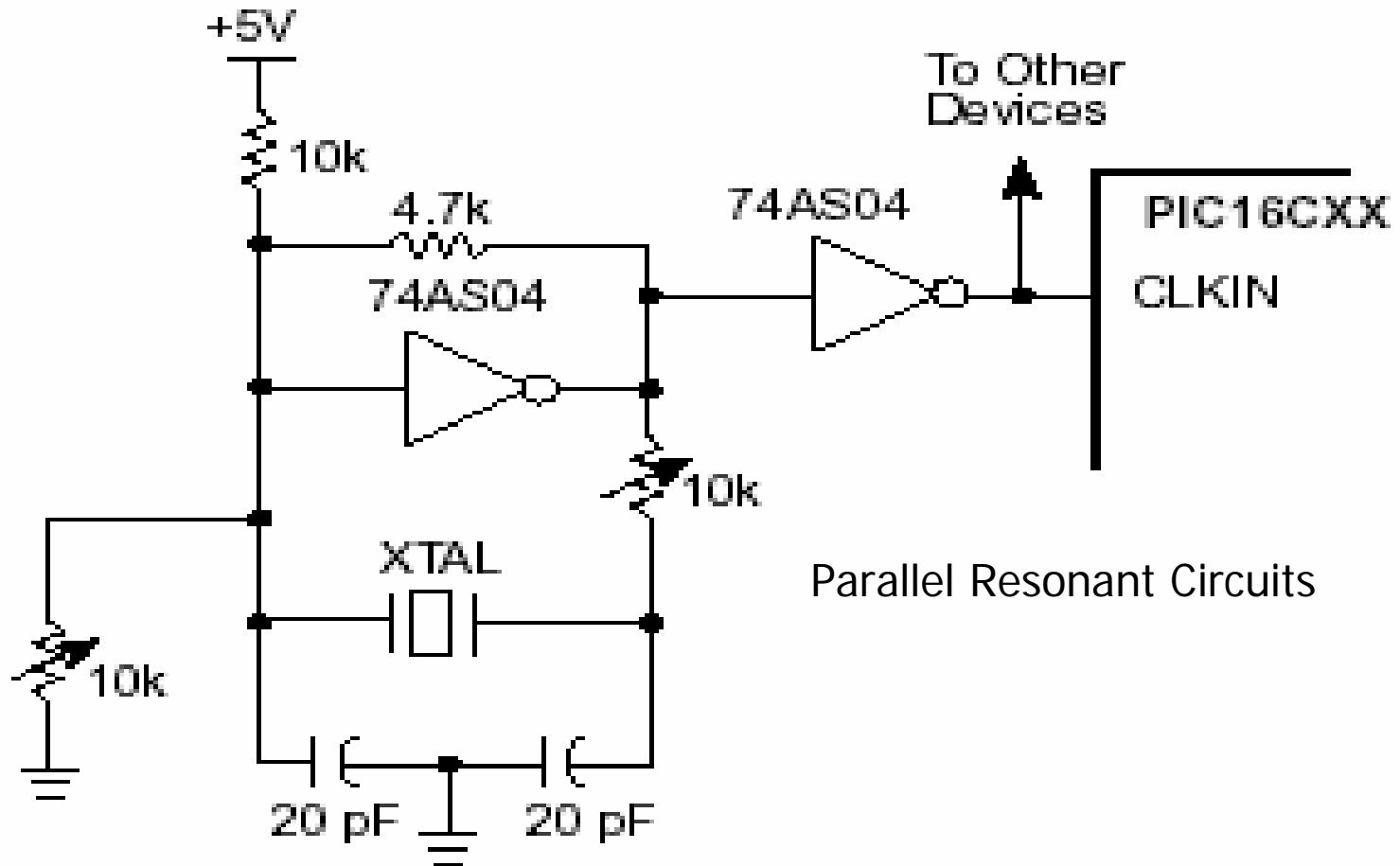
Architecture Contd..

- **PCLATH** (PC Latch)
- Can be independently read or written like any other register.
- It's different from PC and is separate entity.
- It is 5 bits. This is added with PCL (Program Counter Lower) so as to get 13 bit address.

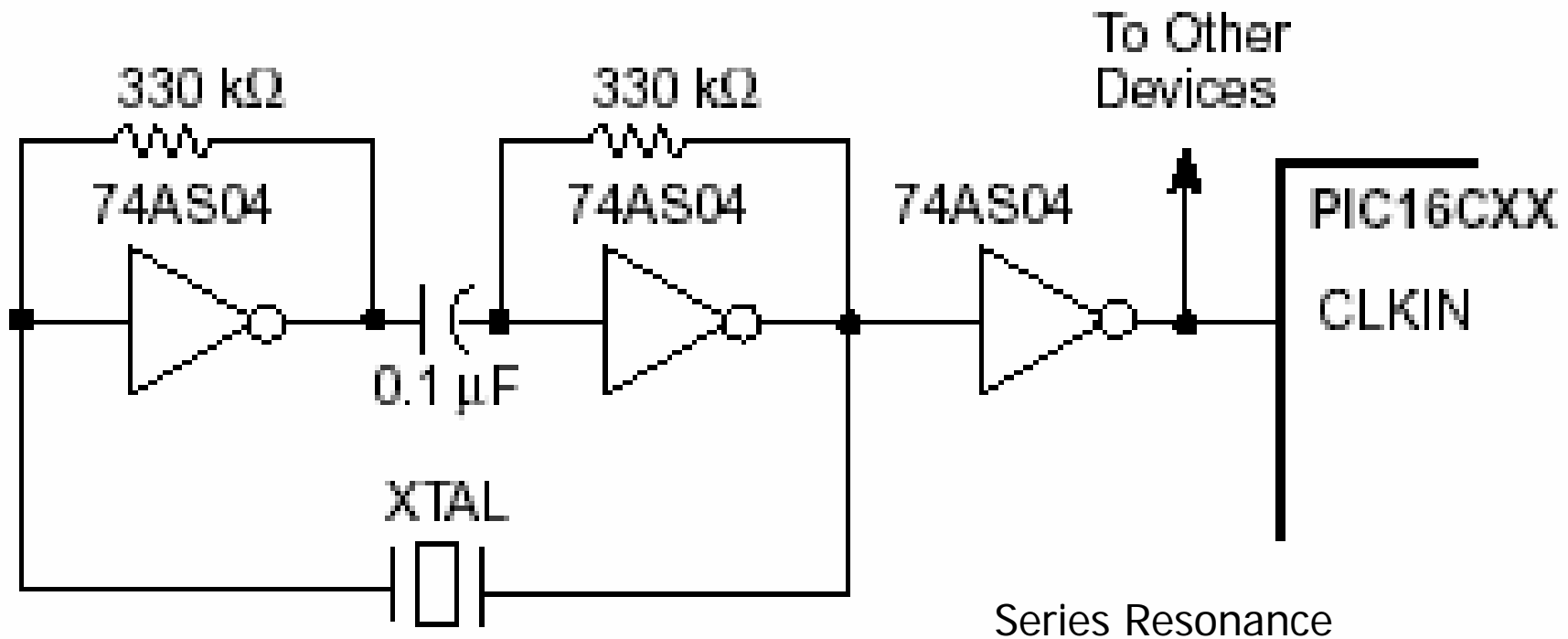
Oscillator Connections



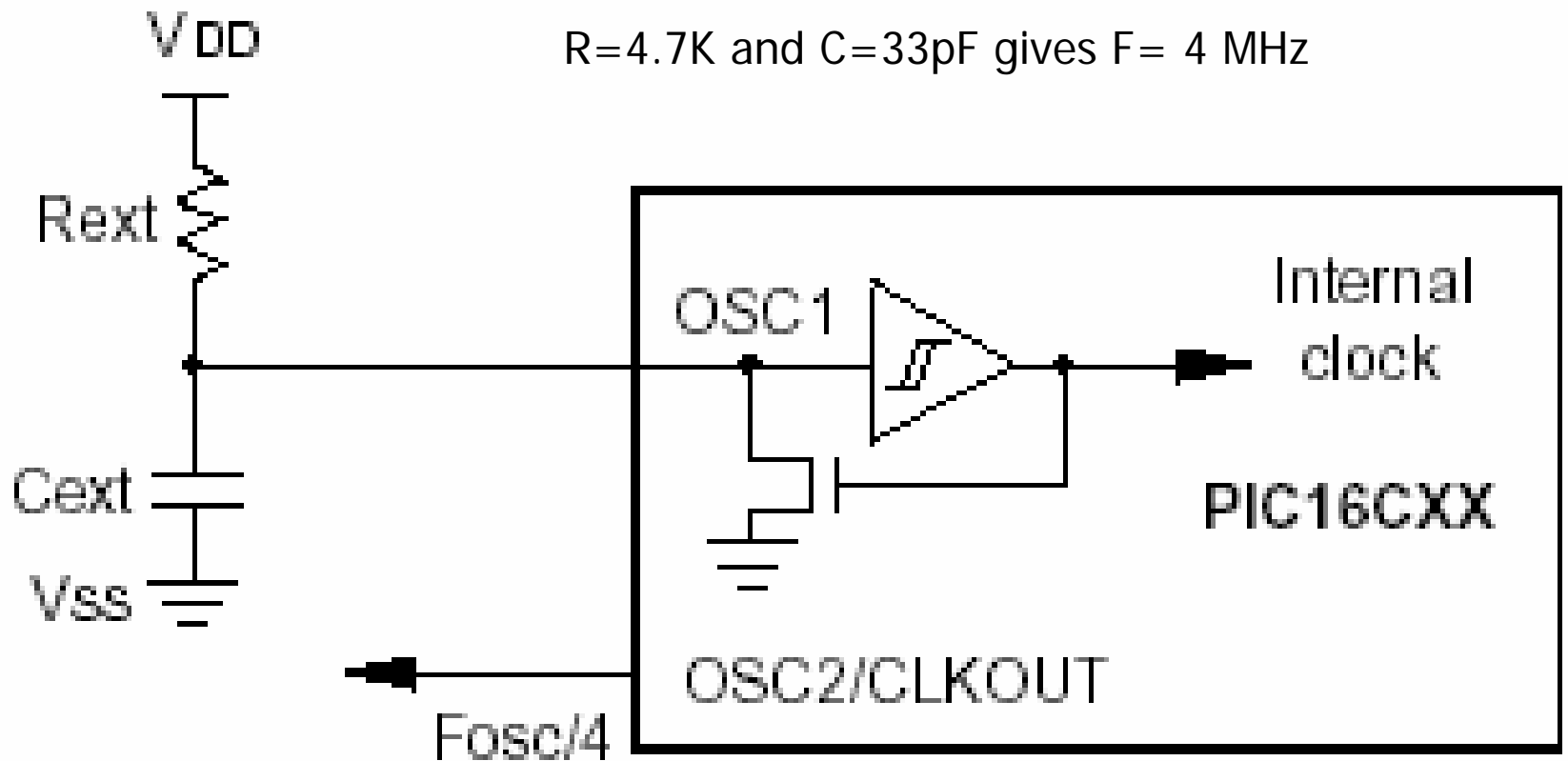
External Oscillator Connections



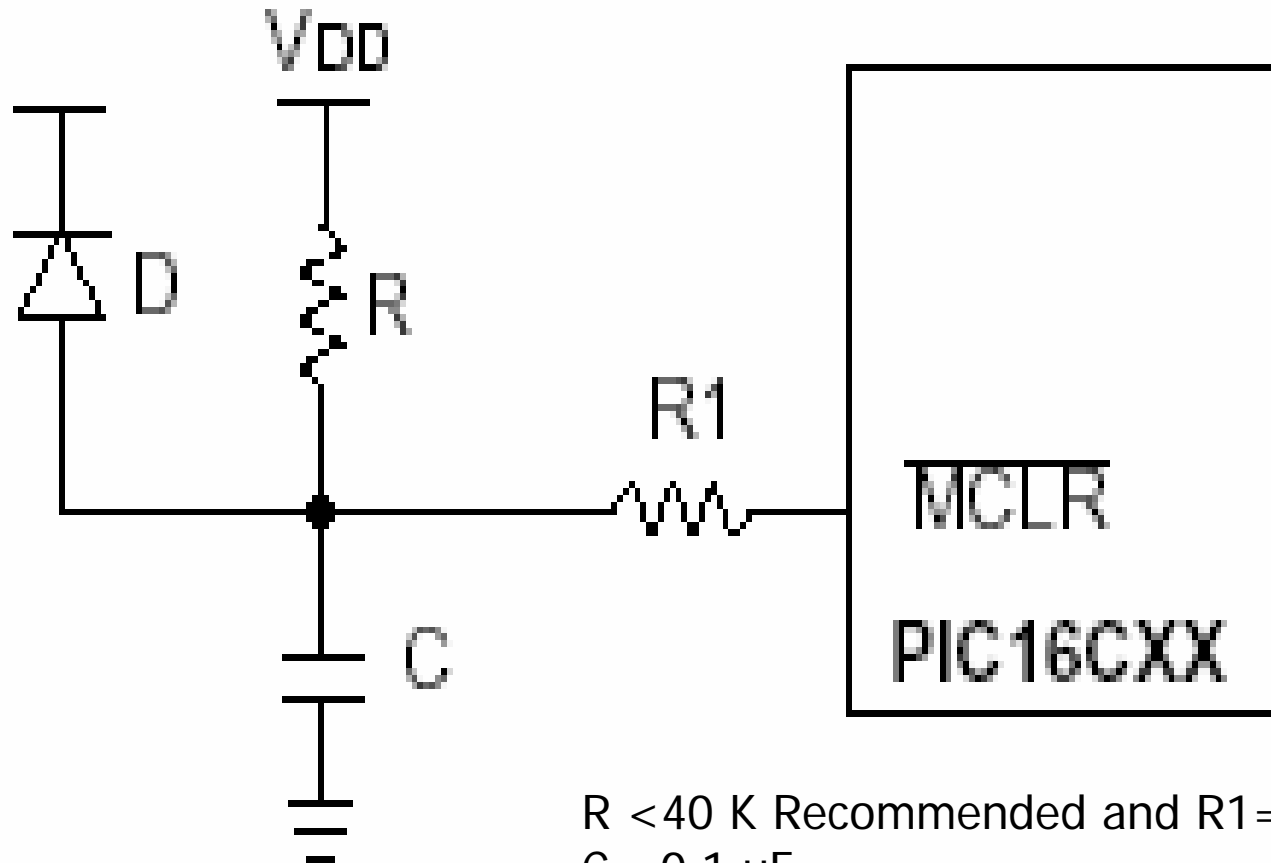
External Oscillator Connections



RC Oscillator Connections

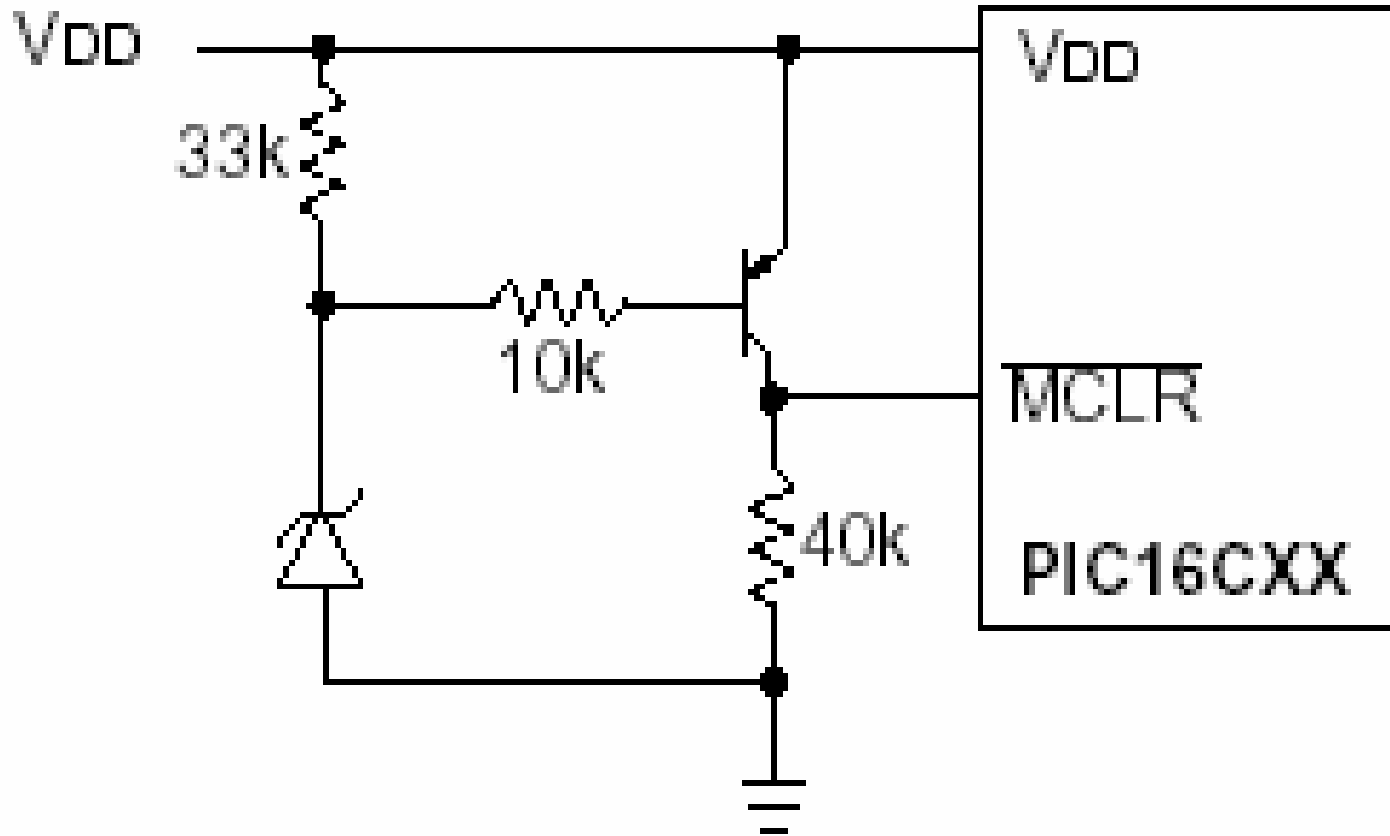


Reset circuitry



$R < 40\text{ K}$ Recommended and $R1 = 100$ to 1K
 $C = 0.1\text{ }\mu\text{F}$

Brown Out Circuitry

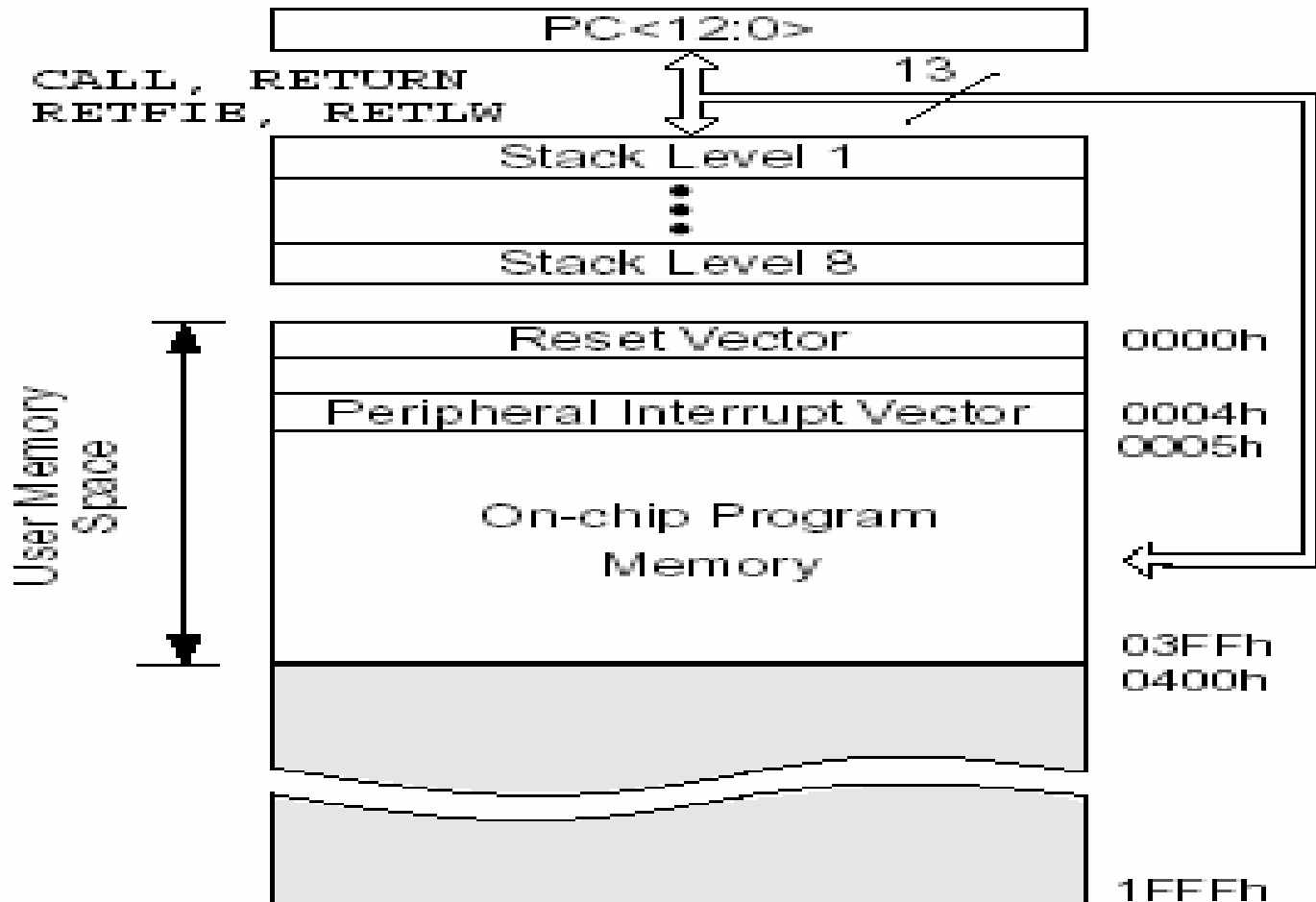




Program Memory

- PIC 16c6X/7X is 2K or 4K.
- 11 bit or 12 bit address is used out of 13 bits in PC.
- Maximum memory that can be accessed is 8K.
- After reset program counter is cleared.
- At 0000h there is "goto Mainline" Instruction which takes PC to 0005h.

Program Memory Contd..





Data Memory

- **Register File Structure.**

They are the memory locations that are addressed by instruction.

There is **general purpose** and **special purpose** register file.

General purpose are 8 bit RAM locations and special purpose are I/O ports and control registers.

File Address

File Address

00h	INDF ⁽⁰⁾	INDF ⁽⁰⁾	50h
01h	TMR0	OPTION	51h
02h	PCL	PCL	52h
03h	STATUS	STATUS	53h
04h	FSR	FSR	54h
05h	PORTA	TRISA	55h
06h	PORTB	TRISB	56h
07h			57h
08h			58h
09h			59h
0Ah	PCLATH	PCLATH	5Ah
0Bh	INTCON	INTCON	5Bh
0Ch	General Purpose Register	Mapped in Bank 0 ⁽²⁾	5Ch
2Fh			AFh
30h			80h
7Fh			Fh

Bank 0

Bank 1

OPTION Register

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7						bit0	

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR reset

- bit 7:** RBPU: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values
- bit 6:** INTEDG: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin
- bit 5:** T0CS: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)
- bit 4:** T0SE: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin
- bit 3:** PSA: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module
- bit 2-0:** PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Please refer P.36 of data sheet.



INTCON register

Please refer p.37 of data sheet.



Addressing Modes

- **Direct Addressing**

It uses 7 bits of instruction and the 8th bit from RP0. If bit is 0 then bank 0 otherwise bank 1.

- **Indirect addressing**

In this mode the 8 bit address of the location in register file to be accessed is written in FSR and use INDF.



I/O Ports

- **Port A**

RA0 to RA4 (5 lines)(Address 05)

RA4 has alternate function. **TRISA(85H)**

is SFR used to configure these lines individually as either inputs or outputs. Setting bit in TRIS will configure as input and 0 will configure as output.

- **Port B**

RB0 to RB7(8 lines).**TRISB**

It has weak internal pull up which is to be enabled. POR disables pull ups.



Interrupts

- **3** Interrupt Sources for 16C61.
- **External Interrupt** –Due to external source.Edge Sensitive RB0/INT causes this interrupt.This interrupt wakes up processor from SLEEP.This must be set before going into SLEEP mode.
- **Timer 0** –Timer 0 overflow. FF to 00 overflow.
- **Port B Change Interrupt** – A change from high to low or low to high on port B pins RB4 to RB7 causes this interrupt.This interrupt can wake device from SLEEP.
- **ADC** – For 16C71 series as EOC.



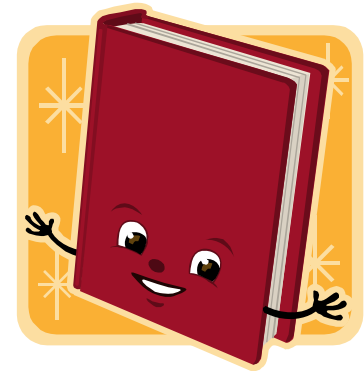
Timers

- 8 Bit wide.
- Clocked internally by system clock which is $F_{osc}/4$ or by external clock on RA4/T0CKI. (Frequency 0 – 50 MHz)
- Incrementing. Overflows from FF-00 and generates interrupt.
- 2 cycle delay after prescaler for purpose of synchronization of external with internal clock.
- $\text{Timer0 delay} = \{ [\text{Timer0 count}] \times \text{Prescaler Value} \times 4 / F_{osc} \}$
- $\text{Timer0 preload} = 256 - [\text{Timer 0 delay} \times F_{osc}] / \text{Prescale value} \times 4]$

Home Work ? ? X



- Watch Dog Timer.
- ADC in 16C71.
- Instruction Set (Interested)
- MPLAB simulation (Interested)



(Ref. Chapter 9 from Micrcontrollers by Ajay Deshmukh, TMH)

Datasheets to be downloaded from Microchip.com



Thank You