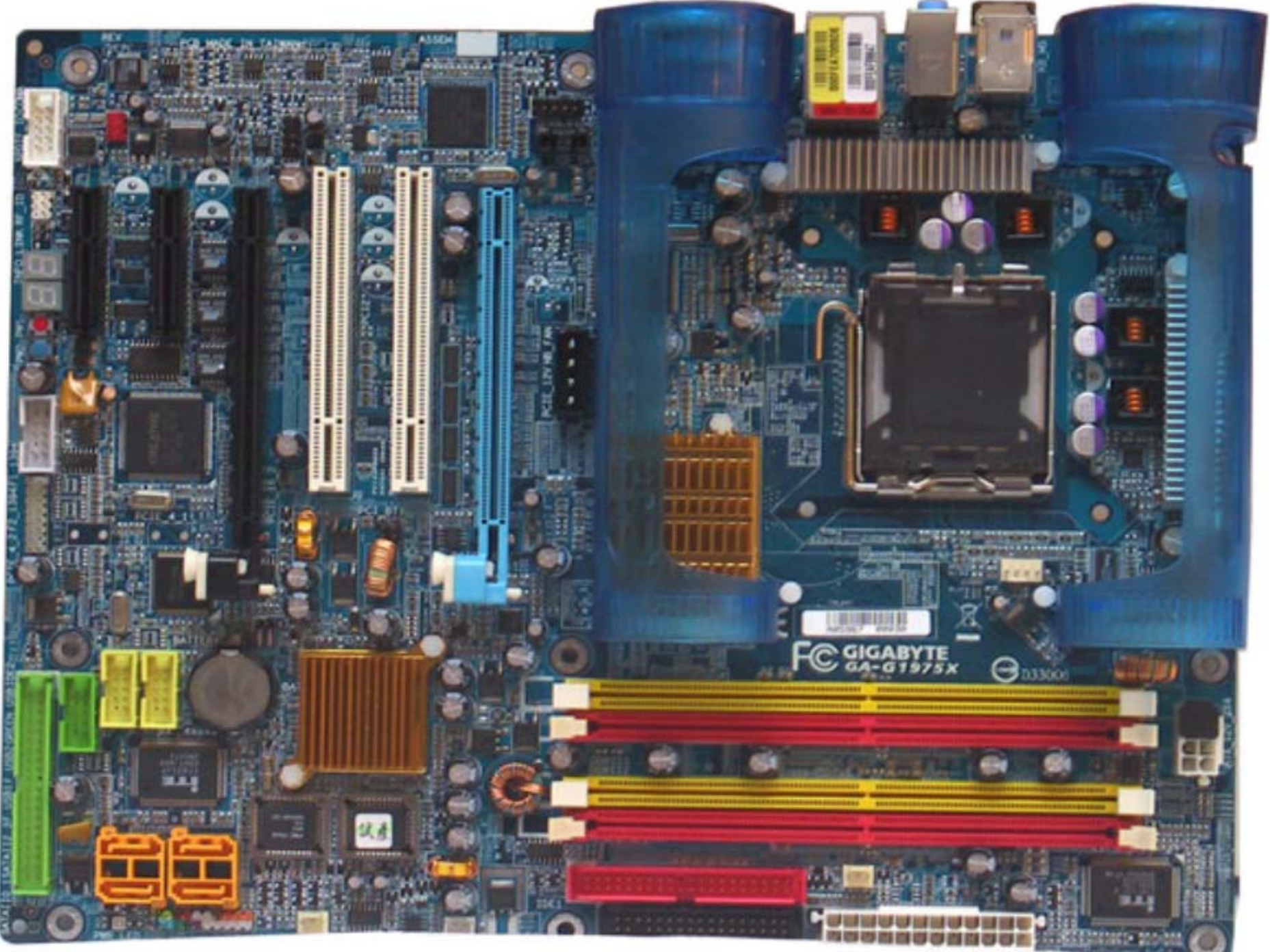




Pentium



FC GIGABYTE
GA-G1975X

D33006



Features of Pentium Processor



- ★ Complex instruction set with RISC features and support for older X86 CPU's.
- ★ Super scalar, super pipelined (4 stage) architecture. (Processors capable of parallel instruction execution of multiple instructions are known as Superscalar. (Two integer or two floating points can be executed Simultaneously).It has two integer pipelines U and V (32 bit each) that enhances the speed of execution.
- ★ It has on chip floating point unit (which is pipelined) that boosts up the performance than 80486.



Features Contd...

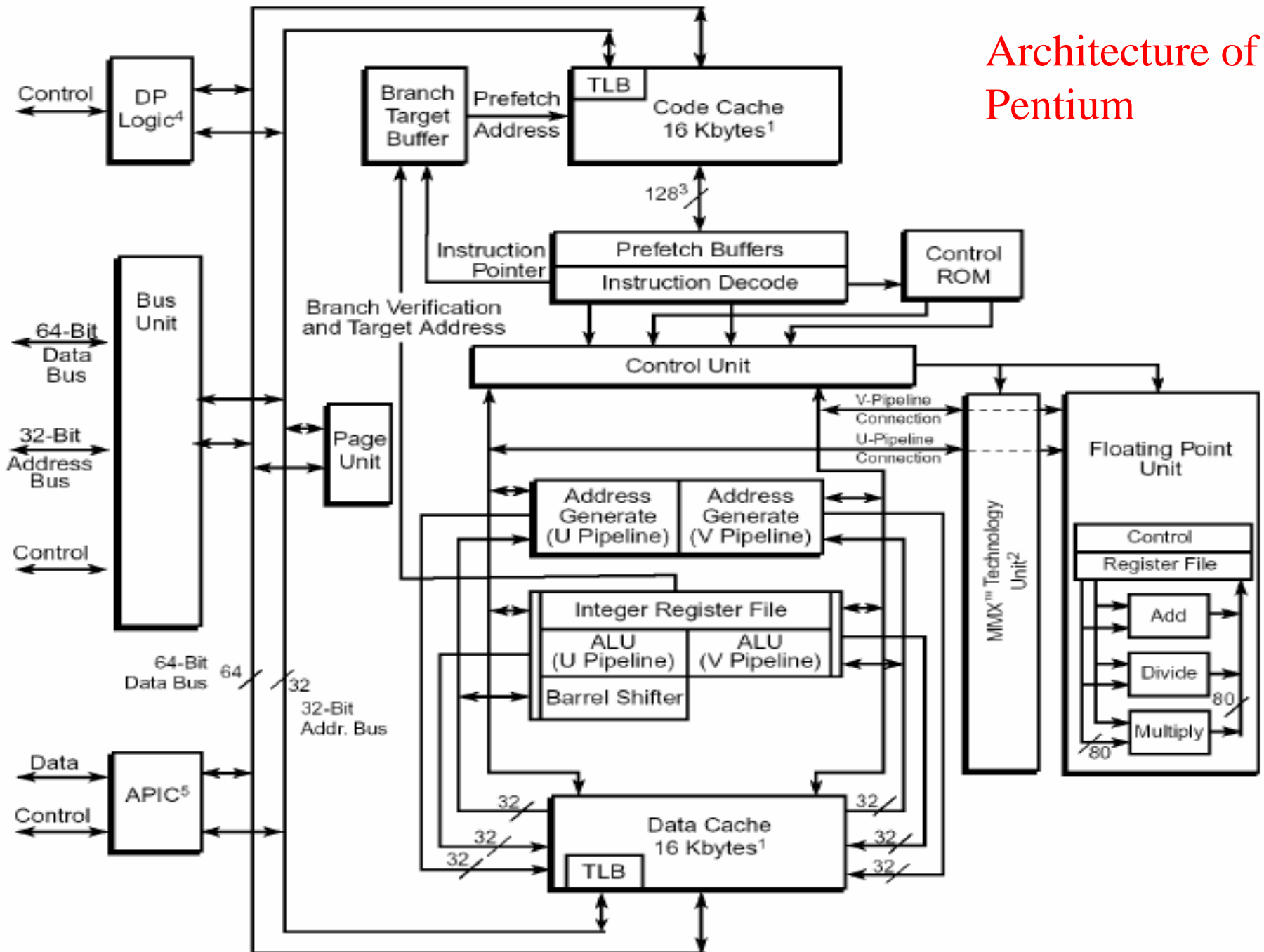
- ★ Two separate cache; 8K for code and 8K for data.
- ★ Dynamic branch prediction.
- ★ Data bus is 64 bit (improves data transfer rate, supports burst read and burst write back cycles).
- ★ Provides high level of data integrity through data parity checking, address parity checking and internal parity checking with machine check exception.
- ★ Test and debug capability through IEEE 1149-1 boundary scan.



Features Contd...

- ★ Virtual mode extensions.
- ★ Operates at 60/66 MHz (5V, 0.8 micron technology), 75/90/100/120/133/150/166/200 MHz (3.3V, 0.6 micron technology). 166 MHz onwards with MMX technology.
- ★ 75 MHz onwards processor offers following enhancements,
 - 1) Dual processing support.
 - 2) Enhanced power management features.
 - 3) On chip advanced programmable interrupt controller (APIC).

Architecture of Pentium





Super scalar Architecture



- ★ The Pentium processor is a superscalar machine, built around two general purpose integer pipelines and a pipelined floating-point unit capable of executing two instructions in parallel. Both pipelines operate in parallel, allowing integer instructions to execute in a single clock in each pipeline.
- ★ The pipelines in the embedded Pentium processor are called the “u” and “v” pipes and the process of issuing two instructions in parallel is termed “pairing.” The u-pipe can execute any instruction in the Intel architecture, whereas the v-pipe can execute “simple” instructions.
- ★ Each of the two pipelines has five stages



Stages of Superscalar



1] Prefetch : Instructions are prefetched from instruction cache or memory.



2] D1 instruction decode : Two parallel decoder works together to decode and generate control signals.



3] D2 Address generate :By decoding the addresses of memory resident operands are calculated.

4] Execute

5] Write Back : In this stage the contents of registers and status flags are updated depending upon instructions..



Branch Prediction

- ★ The Pentium processor uses a Branch Target Buffer (BTB) to predict the outcome of branch instructions, thereby minimizing pipeline stalls due to prefetch delays.
- ★ The processor accesses the BTB with the address of the instruction in the D1 stage. It contains a Branch prediction state machine with four states: (1) strongly not taken, (2) weakly not taken, (3) weakly taken, and (4) strongly taken. In the event of a correct prediction, a branch executes without pipeline stalls or flushes. Branches that miss the BTB are assumed to be not taken.



MMX Technology



- ★ Intel's MMX technology, supported on the Pentium processor with MMX technology, is a set of extensions to the Intel architecture that are designed to greatly enhance the performance of advanced media and communications applications. These extensions (which include new registers, data types, and instructions) are combined with a single-instruction, multiple-data (SIMD) execution model to accelerate the performance of applications such as motion video, combined graphics with video, image processing, audio synthesis, speech synthesis and compression, telephony, video conferencing, and 2D and 3D graphics, which typically use compute-intensive algorithms to perform repetitive operations on large arrays of simple, native data elements.



Contd..



The MMX instruction set consists of 57 instructions, grouped into the following categories:

- ★ Data Transfer Instructions
- ★ Arithmetic Instructions
- ★ Comparison Instructions
- ★ Conversion Instructions
- ★ Logical Instructions
- ★ Shift Instructions
- ★ Empty MMX State (EMMS) Instruction

These instructions provide a rich set of operations that can be performed in parallel on the bytes, words or double words of an MMX packed data type.



Advances in Pentium Technology

★ PENTIUM PRO

★ Features

- 1) It includes L2 cache.
- 2) It uses 12 stage pipeline.
- 3) Supports speculative execution.
- 4) Dual independent Bus.
- 5) Multiple branch prediction.
- 6) Three independent units
 - i) fetch – decode
 - ii) dispatch – execute
 - iii) retrieve unit.



Contd ...

★ **PENTIUM III**

★ **Features**

- 1) 0.25 micron technology.
- 2) 450 MHz/ 500/ 550 up to 1.1 GHz available.
- 3) 70 new instructions used for imaging, speech processing and multimedia applications.
- 4) Dual independent bus.
- 5) 512 Kb unified, non blocking level 2 cache has been used.
- 6) 8, 64 bit wide MMX registers.



Contd ...

★ **PENTIUM 4**

★ Features:

- 1) 0.13 micron technology.
- 2) 1.4 to 1.6 GHz range
- 3) Total 144 SIMD instructions to enhance MM operation.
- 4) 845/850/915/945 chipset.
- 5) 400 /533 MHz system bus frequency.



Home work

- ★ Code and Data Cache.
- ★ Floating point unit.
- ★ Power management in pentium



Ref : Advance Microprocessors by Ray and Bhurchandi, Tata McGraw Hill. Chapter 11.

Thank You