Bansilal Ramnath Agarwal Charitable Trust's

Vishwakarma Institute of Information Technology, Pune-48

(An Autonomous Institute Affiliated to Savitribai Phule Pune University)

Department of Electronics and Telecommunication Engineering

Ph. D Entrance Test

Paper 2: E&TC Engineering

Examination Scheme
Total Marks: 100
(Multiple Choice Questions- 2 marks each)

Unit I: Networks, Signals and Systems
Nodal and mesh analysis; Network theorems: superposition, Thevenin and Norton's, maximum power transfer; Steady state sinusoidal analysis using phasors; Time-domain analysis of simple linear circuits; Solution of network equations using Laplace transform; Frequency domain analysis of RLC circuits; Linear 2-port network parameters: driving point and transfer functions; State equations for networks. Fourier series and Fourier transform representations, sampling theorem and applications; Discrete-time signals: discrete-time Fourier transform (DTFT), DFT, FFT, Z-transform, interpolation of discrete-time signals; LTI systems: definition and properties, causality, stability, impulse response, convolution, poles and zeros, parallel and cascade structure, frequency response, group delay, phase delay, digital filter design techniques.
Unit –II: Electronic Devices
Energy bands in intrinsic and extrinsic silicon; Carrier transport: diffusion current, drift current, mobility, and resistivity; Generation and recombination of carriers; Poisson and continuity equations; P-N junction, Zener diode, BJT, MOS capacitor, MOSFET, LED, photodiode, and solar cell; Integrated circuit fabrication process: oxidation, diffusion, ion implantation, photolithography, and twin-tub CMOS process
Unit III: Analog Circuits
Small signal equivalent circuits of diodes, BJTs and MOSFETs; Simple diode circuits: clipping, clamping and rectifiers; Single-stage BJT and MOSFET amplifiers: biasing, bias stability, mid-frequency small-signal analysis and frequency response; BJT and MOSFET amplifiers: multi-stage, differential, feedback, power and operational; Simple op-amp circuits; Active filters; Sinusoidal oscillators: criterion for oscillation, single-transistor and op-amp configurations; Function generators, wave-shaping circuits and 555 timers; Voltage reference circuits; Power supplies: ripple removal and regulation
Unit IV: Digital Circuits

Number systems; Combinatorial circuits: Boolean algebra, minimization of functions using Boolean identities and Karnaugh map, logic gates and their static CMOS implementations, arithmetic circuits, code converters, multiplexers, decoders and PLAs; Sequential circuits: latches and flip-flops, counters, shift-registers and finite state machines; Data converters: sample and hold circuits, ADCs and DACs; Semiconductor memories: ROM, SRAM, DRAM; 8-bit microprocessor (8085): architecture, programming, memory and I/O interfacing
Unit V : Control System
Basic control system components; Feedback principle; Transfer function; Block diagram representation; Signal flow graph; Transient and steady-state analysis of LTI systems; Frequency response; Routh-Hurwitz and Nyquist stability criteria; Bode and root-locus plots; Lag, lead and lag-lead compensation; State variable model and solution of state equation of LTI systems.
Unit VI: Communication Systems
Random processes: autocorrelation and power spectral density, properties of white noise, filtering of random signals through LTI systems; Analog communications: amplitude modulation and demodulation, angle modulation and demodulation, spectra of AM and FM, super heterodyne receivers, circuits for analogue communications; Information theory: entropy, mutual information, and channel capacity theorem. **Digital communications:** PCM, DPCM, digital modulation schemes, amplitude, phase, and frequency shift keying (ASK, PSK, FSK), QAM, MAP and ML decoding, matched filter receiver, calculation of bandwidth, SNR and BER for digital modulation; Fundamentals of error correction, Hamming codes; Timing and frequency synchronization, inter-symbol interference and its mitigation; Basics of TDMA, FDMA and CDMA.

B.O.S. Chairman
Department of E&TC Engineering